Tufts UNIVERSITY | Department of Computer Science

Class Schedule:

Day	Section	Content
Week 1	***Week 1***	***Week 1***
Wed. May 21	Lecture	Class introduction, overview of the current state of computer architecture, and computer architecture trends. Fundamentals: Dependability and measuring/reporting performance.
	Lab	Introduction to Logisim; building adders
	HW Assigned	HW 1: Read Chapter 1 of CAQA and Chapter 2.5-2.14 in COAD. Exercises from CAQA: 1.8(a-e). Exercises from COAD: 1.6(parts 1,2,3), 2.4 (all parts), 2.10(all parts), 2.11(all parts)
Thurs. May 22	Lecture	The MIPS Instruction Set Architecture (ISA)
	Lab	MIPS assembly language
Week 2	***Week 2***	***Week 2***
Mon. May 26	No Class (Memorial Day)	
Tues. May 27	Lecture	Instruction Set Principles, MIPS instruction format, Procedure calls
	Lab	More MIPS Assembly
Wed. May 28	Lecture	Logic Design and Clocking
	Lab	Design an ALU in Logisim. Clocking in Logisim.
Thurs. May 29	Lecture	**Homework #1 Due.**
	Lab	Components of a processor: ALU, Register File, Memory, Instruction Fetching.
	HW Assigned	HW2: Read Chapter 4.1-4.4 of COAD. Exercises from COAD: 4.1 (all parts), 4.2 (all parts)
Week 3	***Week 3***	***Week 3***
Mon. June 2	Lecture	The Processor: Building a Data Path

Day	Section	Content
	Lab	Putting together a basic (non-pipelined) MIPS CPU.
Tues. June 3	Lecture	Building a Data Path (continued).
	Lab	Putting together a basic (non-piplined) MIPS CPU (continued).
Wed. June 4	Lecture	Pipelining
	Lab	Putting together a basic (non-piplined) MIPS CPU (continued).
Thurs. June 5	Lecture	Pipelining (continued). **Homework #2 Due.**
	Lab	Putting together a basic (non-piplined) MIPS CPU (continued).
	HW Assigned	HW 3: Read Chapter 4.5-4.15 of COAD. Exercises from COAD: 4.13 (all parts), 4.24 (all parts)
Week 4	***Week 4***	***Week 4***
Mon. June 9	Lecture	The Processor: Data and Control Hazards
	Lab	The MIPS pipeline in Logisim.
Tues. June 10	Lecture	Memory Hierarchy: Caches
	Lab	The MIPS pipeline in Logisim.
Wed. June 11	Lecture	Memory Hierarchy: Virtual Memory
	Lab	The MIPS pipeline in Logisim.
Thurs. June 12	Lecture	Memory Hirearchy: Cache Coherence. **Homework #3 Due.**
	Lab	The MIPS pipeline in Logisim.
	HW Assigned	HW 4: Read Chapter 4 in CAQA. CUDA programming assignment
Week 5	***Week 5***	***Week 5***
Mon. June 16	Lecture	Data Level Parallelism. SIMD parallelism and Vector Architectures.
	Lab	GPU Programming
Tues. June 17	Lecture	Data Level Parallelism. Scatter-Gather. SIMD Implementations.
	Lab	GPU Programming
Wed. June 18	Lecture	Data Level Parallelism. GPU architectures. NVIDIA architecture.
	Lab	GPU Programming

Day	Section	Content
Thurs. June 19	Lecture	
	Lab	GPU Programming
	HW Assigned	Final Exam assigned
Week 6	***Week 6***	***Week 6***
Mon. June 23	Lecture	TBA **Homework #4 Due.**
	Lab	TBA
Tues. June 24	Lecture	TBA
	Lab	TBA
Wed. June 25	Lecture	TBA
	Lab	TBA
Thurs. June 26	Lecture	TBA
	Lab	TBA
Fri. June 27		**Final Exam Due, 9am.**