Tufts UNIVERSITY | Department of Computer Science

COMP 140 (Advanced Computer Architecture) Syllabus
Summer 2014

Description and Objective:

Course Website: The course will have a website with announcements, up-to-date schedule changes, labs, and assignments. Material on the website supersedes information in this document. The website address is: ***http://www.cs.tufts.edu/comp/140/***

Textbooks: The main textbook: *Computer Organization and Design, 4th ed., Hennessy and Patterson, 2009.* We will refer to this book as **COAD**. You can find the online edition through the Tufts library, here:

http://app.knovel.com/web/toc.v/cid:kpCODTHSI3

Additional textbook: *Computer Architecture, A Quantitative Approach, 5th ed. Hennessy and Patterson, 2012.* We will refer to this book as **CAQA** You can find the full text online through the Tufts Library:

http://app.knovel.com/web/toc.v/cid:kpCAAQAE11

The texts are frequently-updated and classic, but are also very dense. We will have problem sets from both COAD and CAQA.

Topics Covered:

Fundamentals of Computer Architecture, and the Current State of Computer Hardware

The Processor: Instruction Set Principles

The Processor: Building a Data Path

Instruction Pipelining: Data and Control Hazards

Exploiting Memory Hierarchy: Caches, Virtual Memory

Data-Level Parallelism (Vector, SIMD, and GPU architectures)

Building a MIPS simulator

Prerequisites: COMP 15, COMP 40 (preferred).

Course Attendance: Attending class is mandatory. Because of the compressed schedule and in-class assignments, it is unwise to miss more than a class or two. If you know ahead of time that you will miss a class, please email the instructor.

Course Location:
Halligan 108, 10:45-12:30, M Tu W Th

Professor:
Chris Gregg direct email: cgregg@cs.tufts.edu

The fastest way to get a response to a question is through piazza.com where COMP140 has a course page, we will use the page to post questions and answers. We will not us piazza for posting homework, labs, and other course materials. We will use its discussion forum only. To sign up and access the site please visit: http://piazza.com/tufts/summer2014/comp140

Grade Calculation:
40% Homework Assignments
40% Lab work, class participation
20% Final Exam

Homework Assignments: There will be one homework assignment per week, due on Thursday at the beginning of class, for a total of four assignments. Some assignments will be problem sets from the textbook, and others will be small coding projects, such as a GPU (CUDA or OpenCL) project. The actual assignments are not long, but they can be hard. I also expect that you will read through each textbook chapter — this is not a trivial task, as the chapters can be densely packed with information.

Exam: There will be one take-home final exam for the class, due on Friday, June 27, at 9am.

Labs: About fifty percent of our class time will be spent working on building a simulator for the MIPS Reduced Instruction Set Computer (RISC). I suggest that you bring your own laptop to work on the labs; if some students do not have laptops, we will move to a lab setting where there will be desktop computers.

We will be using two pieces of software a logic simulator (Logism) and a MIPS assembly simulator (MARS). Logisim, and can be downloaded here:

> http://ozark.hendrix.edu/~burch/logisim/

MARS can be downloaded here:

> http://courses.missouristate.edu/KenVollmar/MARS/MARS_4_4_Aug2013/Mars4_4.jar

Logisim and MARS require Java, which you should install on your computer if it isn't already installed.

Academic Integrity: Students should read the Tufts brochure on academic conduct located here .

A few highlights are presented to emphasize importance: Absolute adherence to the code of conduct is demanded of the instructors, teaching assistants, and students. This means that no matter the circumstance, any suspected misconduct must be reported to Tufts University. Students are encouraged to discuss course materials. However, no collaboration is allowed on homework. Specifically you may discuss assignments and projects verbally, but must write up or work on the computer alone.

If any student does not understand these terms or any material outlined in The Academic Code of Conduct it is his/her responsibility to talk to the instructor.

Class Schedule:

Day	Section	Content
Week 1	***Week 1***	***Week 1***
Wed. May 21	Lecture	Class introduction, overview of the current state of computer architecture, and computer architecture trends. Fundamentals: Dependability and measuring/reporting performance.
	Lab	Introduction to Logisim; building adders
	HW Assigned	HW 1: Read Chapter 1 of CAQA and Chapter 2.5-2.14 in COAD. Exercises from CAQA: 1.8(a-e). Exercises from COAD: 1.6(parts 1,2,3), 2.4 (all parts), 2.10(all parts), 2.11(all parts)
Thurs. May 22	Lecture	The MIPS Instruction Set Architecture (ISA)
	Lab	MIPS assembly language
Week 2	***Week 2***	***Week 2***
Mon. May 26	No Class (Memorial Day)	
Tues. May 27	Lecture	Instruction Set Principles, MIPS instruction format, Procedure calls
	Lab	More MIPS Assembly
Wed. May 28	Lecture	Logic Design and Clocking
	Lab	Design an ALU in Logisim. Clocking in Logisim.
Thurs. May 29	Lecture	**Homework #1 Due.**
	Lab	Components of a processor: ALU, Register File, Memory, Instruction Fetching.
	HW Assigned	HW2: Read Chapter 4.1-4.4 of COAD. Exercises from COAD: 4.1 (all parts), 4.2 (all parts)
Week 3	***Week 3***	***Week 3***
Mon. June 2	Lecture	The Processor: Building a Data Path
	Lab	Putting together a basic (non-pipelined) MIPS CPU.
Tues. June 3	Lecture	Building a Data Path (continued).
	Lab	Putting together a basic (non-piplined) MIPS CPU (continued).

Day	Section	Content
Wed. June 4	Lecture	Pipelining
	Lab	Putting together a basic (non-piplined) MIPS CPU (continued).
Thurs. June 5	Lecture	Pipelining (continued). **Homework #2 Due.**
	Lab	Putting together a basic (non-piplined) MIPS CPU (continued).
	HW Assigned	HW 3: Read Chapter 4.5-4.15 of COAD. Exercises from COAD: 4.13 (all parts), 4.24 (all parts)
Week 4	***Week 4***	***Week 4***
Mon. June 9	Lecture	The Processor: Data and Control Hazards
	Lab	The MIPS pipeline in Logisim.
Tues. June 10	Lecture	Memory Hierarchy: Caches
	Lab	The MIPS pipeline in Logisim.
Wed. June 11	Lecture	Memory Hierarchy: Virtual Memory
	Lab	The MIPS pipeline in Logisim.
Thurs. June 12	Lecture	Memory Hirearchy: Cache Coherence. **Homework #3 Due.**
	Lab	The MIPS pipeline in Logisim.
	HW Assigned	HW 4: Read Chapter 4 in CAQA. CUDA programming assignment
Week 5	***Week 5***	***Week 5***
Mon. June 16	Lecture	Data Level Parallelism. SIMD parallelism and Vector Architectures.
	Lab	GPU Programming
Tues. June 17	Lecture	Data Level Parallelism. Scatter-Gather. SIMD Implementations.
	Lab	GPU Programming
Wed. June 18	Lecture	Data Level Parallelism. GPU architectures. NVIDIA architecture.
	Lab	GPU Programming
Thurs. June 19	Lecture	
	Lab	GPU Programming
	HW Assigned	Final Exam assigned

Day	Section	Content
Week 6	***Week 6***	***Week 6***
Mon. June 23	Lecture	TBA **Homework #4 Due.**
	Lab	TBA
Tues. June 24	Lecture	TBA
	Lab	TBA
Wed. June 25	Lecture	TBA
	Lab	TBA
Thurs. June 26	Lecture	TBA
	Lab	TBA
Fri. June 27		**Final Exam Due, 9am.**