Thermal Analysis of Multi-Fin Devices

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***Abstract*— As device dimensions shrink into the nanometer range, power and performance constraints prohibit the longevity of traditional MOS devices in circuit design. FinFETs, a quasi-planar double-gated device, has emerged as a replacement. FinFETs are formed by creating a silicon *fin* which protrudes out of the wafer, wrapping a gate around the fin, and then doping the ends of the fin to form the source and drain regions. Wider finFETs are formed using multiple fins between the source and drain regions.**

While finFETs provide promising electrostatic characteristics, they, like other ultra-thin body nano devices, have the potential to suffer from significant self heating. We study in this paper self heating in multi-fin devices. We first propose a flared channel extension thermal model of each individual fin. We then extend the model to accommodate for multi-fin devices. We analyze several fin geometric parameters (fin width, and (gate) length) and investigate how fin spacing, fin height, gate oxide thickness and gate height affect the maximum fin temperatures in rectangular and flared channel extensions. We provide numerical simulation data to validate our findings. We conclude with developing a novel metric, $METS$ (*M*etric for *E*lectro-*T*hermal *S*ensitivity), for measuring device thermal robustness using electro-thermal simulations and use the metric to investigate device sensitivities in different regions of operation.

Our work is novel as it is the first to address thermal issues within multi-fin devices and develop a metric, $METS$, for evaluating device sensitivities in different regions of operation. The metric, while applied to finFETs, is general and can be applied to any type of device for which coupled electrical and thermal models exist. Furthermore, this work provides an impetus for further research on the emerging area of electro-thermal device and circuit design.

I. Introduction

Next-generation VLSI circuits will be composed of devices with dimensions in the nanometer range (e.g. sub-100nm gate lengths). For many decades, planar devices have been the favorites for both bulk and SOI processing. Planar devices however are susceptible to scaling effects. Subthreshold conduction (e.g. leakage current) is the major hurdle that these devices have yet to overcome. Leakage current stems from decreased oxide thicknesses, higher substrate dopings, and decreased channel lengths. A lowered threshold voltage to obtain better performance at lower operating voltages further exacerbates the leakage problem.

The 2003 International Technology Roadmap for Semiconductors predicts several transistor improvements, including strained Si-channels, ultra-thin bodies, and metallic junctions [1]. It also predicts the move towards double-gate devices which allow more than one gate terminal to control the transistor channel. Among double-gated devices, the finFET, originally dubbed as the folded-channel MOSFET [2], promises better alignment of the double gates. Moreover, finFETs have high current drive and offer substantially better control over leakage and short channel effects.

Like a traditional MOSFET, the finFET is composed of a channel, a source, a drain, and a gate. The channel is embodied in a *fin* protruding out of the wafer plane. The fin is fabricated out of either undoped or lightly doped silicon. The gates of the finFET are created by wrapping the gate material around the three sides of the silicon fin, resulting in self-aligned front and back gates. Figure 1 shows the geometric parameters for a finFET. L_{gate} is the gate length; H_{fin} is the fin height; W_{fin} is the fin width or thickness; t_{ox} is the oxide thickness between the side gates and the fin; t_{ox-top} is the oxide thickness between the top gate and the fin. The width of a finFET is defined as: $W = 2 \times H_{fin}$. FinFET fabrication uses a typical planar fabrication process with several new masks introduced into the process [3]. Hisamoto *et* al. [4] devised one of the first finFET fabrication flows, and several others have improved on it [5]–[8]. The main flow roughly consists of etching a fin out of the silicon wafer, depositing the source and drain, depositing the gate oxides, and finally depositing the gate material.

While providing promising electrostatic characteristics, finFETs, along with other nanoscale devices, pose non-trivial self-heating challenges. We outline some of these challenges.

- Device thermal modeling has consisted mainly of modeling a device as a transient three-dimensional heat flow problem [9], [10]. The temperature at any point within the device can be found at any instant in time. The heat diffusion equation however fails to capture the dominant thermal energy transport mechanism due to phonons, particles that transport energy, and atomic lattice vibrations. Recently, the Boltzmann Transport Equation (BTE) was used to estimate the hot spots associated with the drain regions [11], [12]. For example, Sverdrup, Ju, and Goodson compared the BTE to classic heat diffusion temperature estimations within a MOSFET device. They found the heat diffusion equation underestimates the maximum device temperature, when compared to BTE estimates, by as much as 159% [11].
- The small and confined dimensions of the fin reduce the thermal conductivity (which increases the thermal resistance) of the device due to reduced phonon mean path [13]. Heat transport out of the device is hindered, and the device temperature rises.
- Heat dissipation is sensitive to the dimensions of source and drain extensions [14]. Careful device thermal analysis is needed to balance the device's electrical characteristics with thermal ones [5].
- SOI finFETs are even more susceptible to self heating than bulk ones: SOI thermal conductivity is two orders of magnitude less than that of silicon [15].
- FinFET thermal problems are further exasperated with the construction of wider finFETs built using parallel

fins between the source and the drain areas, as shown in Figure 2 [16]. These fins are tightly laid out. Heat removal from the middle fins is not as efficient as the removal from the end fins.

With the potential impact of temperature on performance and reliability, thermal device design becomes important, specially for analog circuits. Jenkins and Franch recently investigated how self heating in SOI CMOS circuits affects worst-case drain current [17]. Our paper studies the effects of steady-state self-heating in multi-fin devices. Our investigation is based on the ultra-thin body (UTB) SOI thermal model introduced by Pop, Dutton, and Goodson [14]. We first propose a flared channel extension thermal model of each individual fin. We then extend that model to account for multiple-fins. By carefully examining the multi-fin model, we are able to identify the key parameters that affect the maximum temperatures within multi-fin devices. Our numerical simulation data validates our parameter choices. We then introduce our thermal sensitivity metric, *METS*, and investigate device sensitivities in different regions of operation. Our findings can be used to guide the design of optimal finFET devices, and to drive thermal-aware transistor and circuit-level optimizations.

The rest of the paper is organized as follows. We review device thermal analysis in Section II and propose our single-fin flared channel extension thermal model in Section II-A. In Section III, we model multi-fin devices and discuss critical design parameters in the thermal design of these devices. We then introduce our electro-thermal simulation methodology in Section IV. We provide experimental results in Section V and our *METS* metric in Section V-E. We describe some limitations of this work, and conclude with future research directions that highlight the role of thermal device modeling and its implication on circuit design.

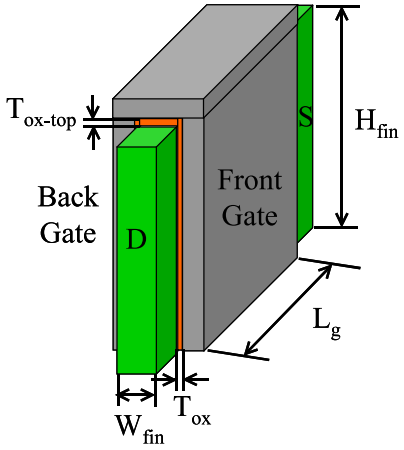


Fig. 1. FinFET device.

II. Background: Thermal Analysis for Single-Fin Devices

Heat generated in n-type transistors is due to electron-phonon interactions in the drain region. When a device is turned on, free electrons in the source are accelerated through the channel to the drain region. This acceleration causes the electrons to gain energy as they move through the channel. Once in the drain region, electrons are free to scatter with other electrons, phonons, impurity atoms, etc. Electron-phonon scattering results in an energy exchange between the electrons and the lattice which causes the lattice temperature to increase (other scattering mechanisms change electron momentum, but not energy) [19]. While electron-phonon scattering may occur in other regions of the device, any heat generated from the scattering produces an insignificant amount of heat generation when compared to the drain region.

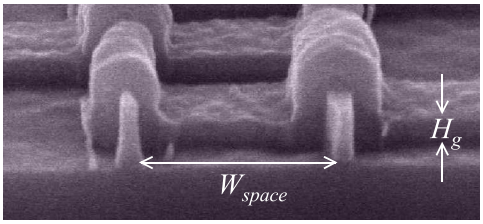


Fig. 2. Multi-fin device [18].

Heat generated in the drain region of a finFET device causes a temperature gradient within the device. A detailed discussion of heat generation within transistors can be found in [19], [20]. An approximation of the generated heat (Watts) is:

$$Q = I_D \cdot V_{DS} \tag{1}$$

The relationship between heat and temperature is governed by Fourier's law of heat conduction. This is illustrated in Figure 3, where the boundary condition T_0 has been applied to the surface on right-hand side of the block. Fourier's law is:

$$\Delta T = \frac{L}{k \cdot A} \cdot Q \tag{2}$$

where ΔT is temperature difference, L is the length of the heat conduction, k is the thermal conductivity of material in the heat conduction path, A is the cross sectional area of heat conduction, and Q is the heat.

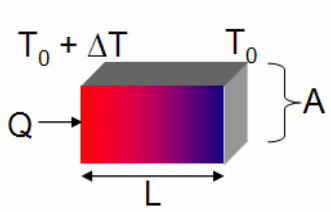


Fig. 3. Illustration of Fourier's law of heat conduction.

The electrical analogy of Fourier's law is Ohm's law. When heat is applied to a solid, a temperature gradient forms across the solid. This relationship is mathematically identical to an electrical current creating a voltage difference across and electrical resistor when forced through the resistor. If substitutions are made in equation (2) such that $\Delta T = \Delta V$, $Q = I$, and $L/kA = R$, the equation appears in the form of Ohm's law, $\Delta V = R \cdot I$. The equivalence between Fourier's law and Ohm's law is useful. Heat transfer analysis involving

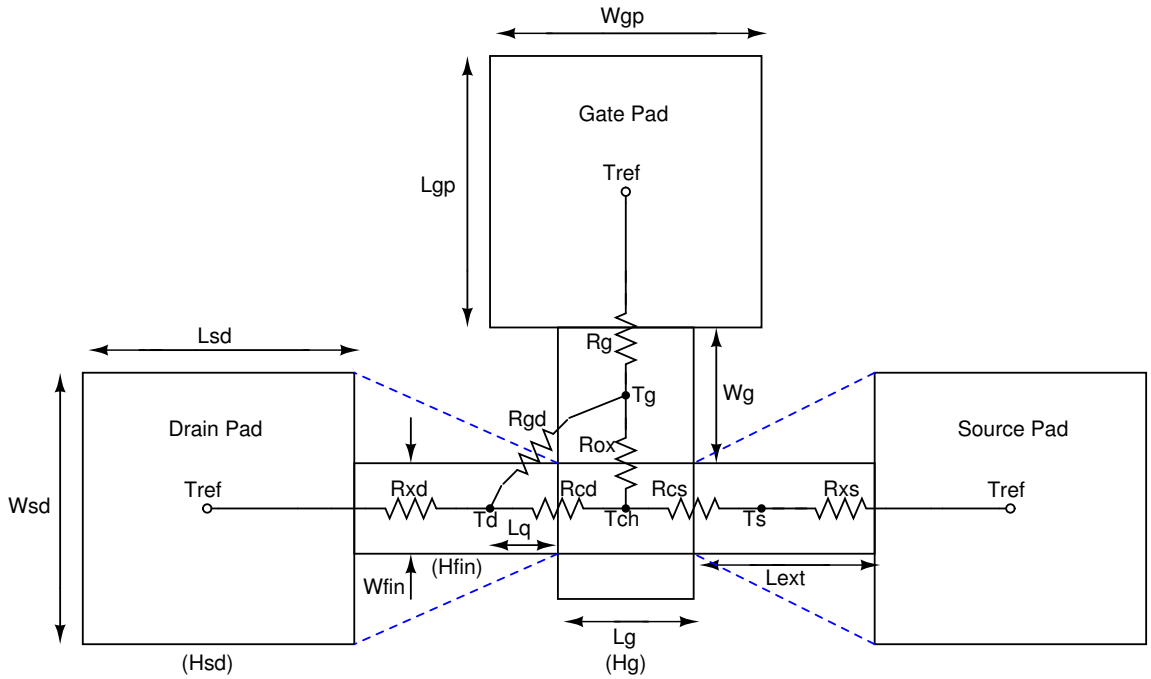


Fig. 4. Top view of a finFET layout with equivalent thermal resistances [14]. The dotted lines represent flared channel extensions. Markings with () signify height dimensions. Only one gate pad is used in this analysis.

complicated geometries can be simplified by identifying select points within the geometry where temperatures are to be calculated. SPICE can then be used to solve for node voltages (i.e. temperatures) in the thermal network [21].

Pop *et* al. introduced a thermal model for an ultra-thin body SOI (UTB-SOI) device using the thermal-electrical equivalence [14]. The model uses a reduced thermal conductivity to account for the thin device geometry and impurity effects on the phonon mean free path. While not accounting for all thermal nano concerns, the model can be applied to devices with different gating structures, including finFETs. We refer to this model as the UTB model in the rest of the paper.

An ultra thin device and its equivalent UTB model are respectively shown in Figure 4 and in Figure 5. The gate, drain, and source pads are assumed to connect through metal contacts to other circuit elements. Their top surface is assumed to be at a reference temperature[1]. Adiabatic boundary conditions are applied to all other surfaces. Thus heat only flows in and out of the device at the top surface of the pads. Equivalent resistances are calculated using the formula $R = L/kA$, based on the materials and geometries through which heat transfer occurs. The current source representing the heat Q can be applied to the UTB model at the drain node since it is the heat generation region. The injected current can be calculated using (1). Circuit analysis can then be used to solve for the temperatures at the drain, source, channel, and gate. Pop *et* al.'s findings showed that the device temperatures are most sensitive to the drain pad and channel extension dimensions.

[1]If the individual pad temperatures are known, the thermal model can be adjusted according by adding voltage sources between the source/drain/gate nodes and the reference temperature.

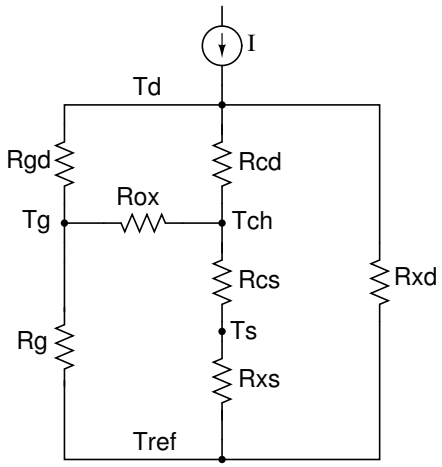


Fig. 5. Pop's equivalent thermal circuit [14].

A. Single-Fin Thermal Model Enhancement: Flared-Channel Extensions

FinFET device performance is dependent on source and drain channel extension layout [22]. Flared channel extensions, as opposed to rectangular channel extensions, can be used to decrease parasitic source and drain channel extension resistance, hence improving I_{on}. As fin thicknesses decreases, flared fins become more important in enhancing device performance. We enhance the UTB thermal model to account for flared channel extensions.

Figure 4 shows two dashed lines on either side of the channel extension, representing the flared channel extension. We alter the source and drain channel extension thermal resistances (R_{xd} and R_{xs}) to properly model heat flow through

the channel extension region. The channel extension region is sliced into *m segments* from pad to channel and the thermal resistance of each segment is computed. The equivalent channel extension thermal resistance is the total series resistance the *m segments*. Detailed flared-channel extension calculations will be shown in Section III.

III. Multi-Fin Thermal Model

To model wider finFETs with multiple fins, the equivalent thermal circuit model described in Section II is modified as follows. We assume that fins are spaced a distance W_{space} apart, and that there will be two gate pads, one on each side of the outside-most fins. If an instance of Figure 5 is used for each fin, only these outer fins can have the resistor R_g. An open circuit replaces R_g for all inner fins. Furthermore, gate nodes of adjacent fins will be connected by an inter-gate thermal resistance, R_i, representing the heat flux path between fins through the poly gate. This inter-gate resistance R_i is calculated using $R = L/kA$ where L is the fin separation W_{space}, k is the thermal conductivity of polysilicon, and A is the cross sectional area of heat flow through the gate poly. Figure 6 shows an example thermal circuit of a 3-fin device. Heat injection occurs within the drain region for each fin.

To understand the effects of multi-fin device geometry on thermal characteristics, we analyze the equations used to generate the thermal resistance values. The thermal resistance from the source node to the source-side metal contact, R_{xs}, is dependent on the fin extension length and the size of the source pad. The resistance is computed as two series resistances. The first one is through the fin with the cross section of $W_{fin} \times H_{fin}$. The second resistance is between the fin and the top of the source pad. The heat flux in this region bends upwards from the area where the fin (cross section area of $W_{fin} \times H_{fin}$) meets the pad (cross section area of $L_{sd} \times H_{sd}$) to the metal on the top face of the pad. We assume that the length of the resistive path is about half of the length of the source pad, and that the cross section area of the path is the average of the two areas. The resistance R_{xs} is then computed as:

$$R_{xs} = \frac{L_{ext}}{k_{ext} \cdot (W_{fin} \cdot H_{fin})} + \frac{L_{sd}}{k_{sd} \cdot (W_{fin} \cdot H_{fin} + L_{sd} \cdot H_{sd})} \quad (3)$$

The use of flared channel extensions alters R_{xs}. The channel extension flare is assumed to start at the channel region and flare out the entire source/drain pad width as the dashed lines in Figure 4 shows. Slicing the channel extension region into *m segments* yields a new R_{xs}, which is computed as:

$$\begin{aligned} R_{xs\_flare} &= \frac{L_{sd}}{2 \cdot k_{sd} \cdot (L_{sd} \cdot H_{sd})} \\ &\quad + \frac{L_{ext}}{m \cdot k_{ext} \cdot H_{fin}} \sum_{i=1}^{m} \frac{1}{W_{fin} + \frac{2 \cdot i \cdot L_{ext} \cdot sin(\theta)}{m}} \\ &where: \\ \theta &= tan^{-1}\left(\frac{W_{sd} - W_{fin}}{2 \cdot L_{ext}}\right) \end{aligned} \quad (4)$$

The thermal resistance from the drain temperature node to the drain-side metal contact, R_{xd}, is dependent on the fin extension length as well as L_q. The latter parameter represents the centroid of heat generation region in the drain region [14]. It is the distance within the drain side of the fin from the edge of the gate[2]. R_{xd} is then computed as:

$$R_{xd} = \frac{L_{ext} - L_q}{k_{ext} \cdot (W_{fin} \cdot H_{fin})} + \frac{L_{sd}}{k_{sd} \cdot (W_{fin} \cdot H_{fin} + L_{sd} \cdot H_{sd})} \quad (5)$$

Similar to the source-side flared channel extension region, R_{xd} is dependent on the number of segments (m) the region is sliced into, and computed as:

$$\begin{aligned} R_{xd\_flare} &= \frac{L_{sd}}{2 \cdot k_{sd} \cdot (L_{sd} \cdot H_{sd})} \\ &\quad + \frac{L_{ext}}{m \cdot k_{ext} \cdot H_{fin}} \sum_{i=n'}^{m} \frac{1}{W_{fin} + \frac{2 \cdot i \cdot L_{ext} \cdot sin(\theta)}{m}} \\ &where: \\ \theta &= tan^{-1}\left(\frac{W_{sd} - W_{fin}}{2 \cdot L_{ext}}\right) \\ n' &= \lfloor \frac{L_q \cdot m}{L_{ext}} \rfloor \end{aligned} \quad (6)$$

The thermal resistance from the center of the channel to the source thermal node, R_{cs} is a function of half of the channel length:

$$R_{cs} = \frac{\frac{1}{2}L_g}{k_{ch} \cdot (W_{fin} \cdot H_{fin})} \quad (7)$$

R_{cd}, the thermal resistance from the center of the channel (T_{ch}) to the drain thermal node (T_d), is a series resistance of two resistances one involving half the channel length and the other involving the distance L_q.

$$R_{cd} = \frac{\frac{1}{2}L_g}{k_{ch} \cdot (W_{fin} \cdot H_{fin})} + \frac{L_q}{k_{ext} \cdot (W_{fin} \cdot H_{fin})} \quad (8)$$

Flared channel extensions alter the thermal resistance between the the heat generation region L_q and the channel region under the gate edge. R_{cd} becomes R_{cd_flare} and is computed as (when the channel extension is cut into m segments):

$$\begin{aligned} R_{cd\_flare} &= \frac{\frac{1}{2}L_g}{k_{ch} \cdot (W_{fin} \cdot H_{fin})} \\ &\quad + \frac{L_{ext}}{m \cdot k_{ext} \cdot H_{fin}} \sum_{i=1}^{n'} \frac{1}{W_{fin} + \frac{2 \cdot i \cdot L_{ext} \cdot sin(\theta)}{m}} \\ &where: \\ \theta &= tan^{-1}\left(\frac{W_{sd} - W_{fin}}{2 \cdot L_{ext}}\right) \\ n' &= \lfloor \frac{L_q \cdot m}{L_{ext}} \rfloor \end{aligned} \quad (9)$$

Equation (10) shows the thermal resistance between the channel and the gate due to the gate oxide. It is dependent on the oxide thickness, and also on R_{if}, which is the interface resistance [14]. R_{if} is independent of processing conditions and accounts for subtle boundary effects at the gate/oxide interface [14]. We assume that t_{ox} is the same as t_{ox-top}.

$$R_{ox} = \frac{1}{L_g(2 \cdot H_{fin} + W_{fin})}\left(R_{if} + \frac{t_{ox}}{k_{ox}}\right) \quad (10)$$

[2] A heat generation region is not present in the source, therefore L_q only appears in drain side thermal resistance calculations.

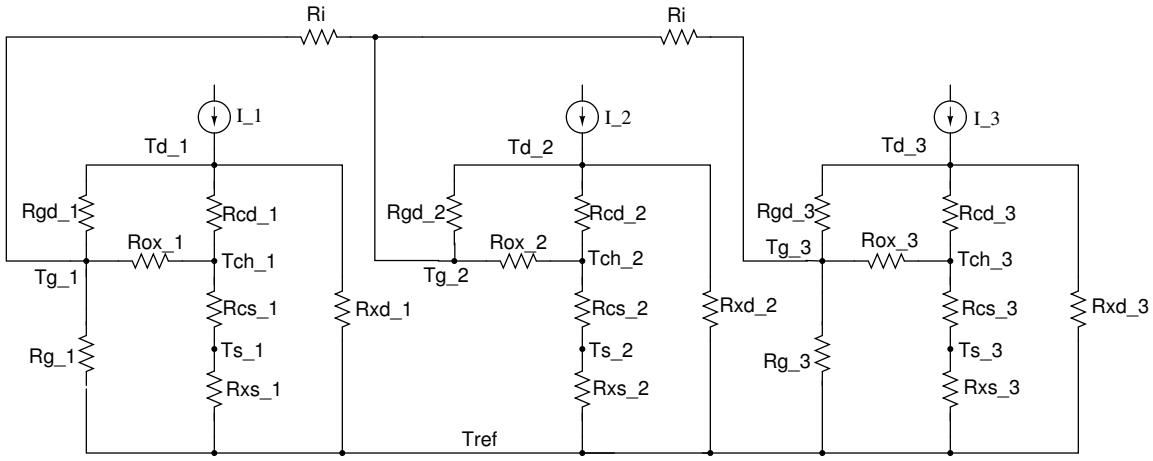


Fig. 6. The equivalent thermal circuit for a 3-fin finFET. All source, drain, and gate pads are at the reference temperature (T_{ref}). All nodes and temperatures are indexed with $\_n$, where n is the fin number (e.g. 1-3). The middle fin (index 2) gate resistance (R_g) is replaced by the inter-gate thermal resistance R_i.

R_g, the thermal resistance between the gate poly at T_g and the gate pad, is dependent on the distance of the gate pad from the fin (W_g):

$$R_g = \frac{W_g}{k_g \cdot (L_g \cdot H_g)} + \frac{L_{gp}}{k_g \cdot (L_g \cdot H_g + L_{gp} \cdot H_g)} \tag{11}$$

Equation (12) shows the thermal resistance between the heat generation region T_d and the gate temperature node. The thermal conduction path is through the oxide surrounding the device, which must be included due to the high temperature difference expected between drain and gate. A gate to source thermal resistance can be neglected due to the low temperature difference between the two regions and the small thermal conductivity of the oxide between the two regions.

$$R_{gd} = \frac{L_q}{\frac{1}{2} \cdot k_{ox} \cdot W_{fin} \cdot H_g} \tag{12}$$

Finally, the inter-fin gate resistance R_i is calculated as follows, where W_{space} is the spacing distance between two consecutive fins, H_g is the gate height, and L_g is the gate length[3]:

$$R_i = \frac{W_{space}}{k_g \cdot H_g \cdot L_g} \tag{13}$$

R_i, is likely to have a significant impact on the heat removal mechanism from the middle fins. It is directly proportional to W_{space}, and inversely proportional to H_g and L_g. For the middle fins, two ways are possible for heat removal: through the source/drain pads, and through the gate.

The high thermal conductivity of the gate material provides the least resistive path for heat to flow out of the device. However, the small thermal conductivity of the oxide restricts heat flow from the channel to the gate. The small thermal conductivity of oxides (side, top, and buried) forces the heat to flow out of the source/drain extensions to the pads. Heat which does reach the gate material is free to spread throughout the device and exit through the gate pad.

[3]The gate-to-substrate thermal resistance is omitted from the model due to the small thermal conductivity of the underlying buried oxide.

Further examination of the equations above, it is clear that the fin cross section, $H_{fin} \times W_{fin}$ affects most of the resistances. We thus suspect that the following six parameters can affect the thermal behavior: H_{fin}, W_{fin}, L_g, W_{space}, T_{ox}, and H_g. We conducted several detailed experiments in Section V to quantify these effects.

IV. Electro-Thermal Device Analysis

Heat applied to the thermal circuit in Figure 5 is dependent on the current flowing through the device as equation (1) describes. However, the current flowing through the device is dependent on the device source temperature, due to the temperature dependence of mobility and threshold voltage. The source temperature controls carrier injection into the channel and ultimately limits the current flowing through the device [14], [23]. This leads to the natural mutual coupling of the electrical and thermal networks.

Electro-thermal simulation has been studied over the past several decades, with numerous approaches. The majority of these works target full chip electro-thermal simulations, requiring reduced thermal networks and/or simplified electrical models [24]–[29]. Unlike these target applications, we are interested in detailed device-level electro-thermal device analysis for finFETs. We have borrowed previous electro-thermal analysis techniques from Liu *et* al. and Chiang *et* al. [30], [31]. Liu *et* al. constructed electro-thermal device models which are thermally compensated for self heating by altering carrier mobility and threshold voltage using an RC equivalent thermal circuit. Chiang *et* al. used SPICE to solve a 3-D distributed thermal circuit model for interconnects. Their model accounts for interconnect self-heating and heat spreading to neighboring interconnects and layers.

Our electro-thermal methodology uses the electro-thermal simulation setup shown in Figure 7 and updates all electrical temperature sensitive parameters, mainly mobility and threshold voltage, at every transient time step in SPICE[4]. We couple

[4]The finFET electrical models used in this work, BSIMDG [32], were obtained from Device Research Group at the University of California, Berkeley.

the electrical and thermal circuits together through dependent sources, and then perform SPICE simulations. Our electro-thermal simulations allow us to simultaneously: (1) model the temperature effect within each fin on its current, and (2) model the effect of current change on the temperature of each fin. We thus produce accurate drain, gate, source, and channel temperature estimations for each fin of a device while taking into consideration the exact location of the fin within a multi-fin device. In Section V we show that this electro-thermal simulation is essential in avoiding the overestimation of the maximum fin temperatures and in accurately estimating the current in in multi-fin devices.

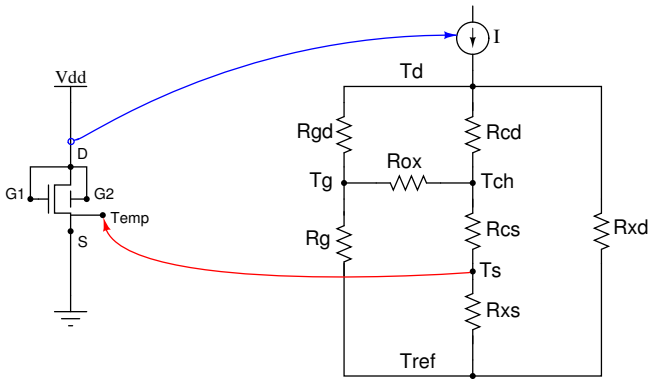


Fig. 7. The equivalent electro-thermal finFET model.

V. Experimental Results

Our goal is to evaluate the electro-thermal characteristics of multi-fin devices. Our baseline (nominal) device is a single fin with the parameters shown in Table I[5]. Our data, when normalized, is in reference to this single-fin case. We first show the temperature and current profile of multi-fin device obtained using electro-thermal simulations. We then examine the temperature and current characteristics in rectangular and flared channel extensions. We then vary the fin geometries and investigate the impact of gate length and height, and fin width, height, and spacing on the temperature and performance of a multi-fin devices. Finally, we investigate the impact of temperature variations on device performance to obtain a thermal sensitivity metric. The experimental data presented herein uses adjusted model parameters with the electro-thermal simulation setup shown in Figure 7; thus creating a new electrical and thermal device for each parameter under investigation.

A. Multi-Fin Electro-Thermal Studies

Using the multi-fin thermal model with electro-thermal simulations we examine: fin temperatures and currents. We also compare the temperature of multi-fin devices with rectangular and flared channel extensions.

[5]The thermal conductivities (k_{xx}) capture the reduced phonon mean free path due to thin device geometries and impurity effects based on Pop *et* al.'s findings [14].

1) Multi-Fin Temperature Profiles in Rectangular Channel Extension Devices: We construct multi-fin devices assuming a fin spacing, W_{space}, of 100nm. A plot of temperature rise (above ambient) for each fin of a 50-fin device is shown in Figure 8. Several observations can be made. First, the inner fins are hotter than outer ones, for the drain, source, gate, and channel. Each fin has the same access to the source/drain pads; however, the gate pads at the reference temperature are further away from the inner fins. This is also the cause for the gate temperature for the inner fins to be hotter than the channel temperature. The gate pads are effective at removing the heat from the gates for outer fins, but less so for the inner fins. Second, for the majority of inner fins, the temperature is relatively constant from one fin to the next. Thus, beyond a certain number of fins, adding more fins to a device will no longer increase the peak temperatures. Third, the drain temperature is the hottest, and the coolest is the source. However, the drain temperature, while the hottest part of the finFET, has the smallest variation across the fins.

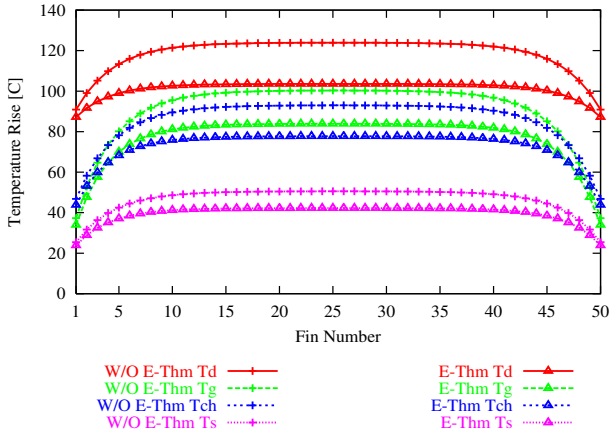


Fig. 8. Temperature profile at the source (T_s), channel (T_{ch}), gate (T_g), and drain (T_d), for a 50-fin device. We show the temperatures obtained with (E-Thm) and without (W/O E-Thm) electro-thermal simulations.

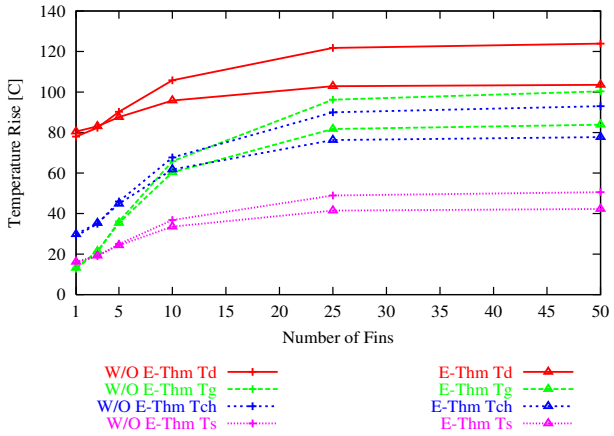


Fig. 9. Temperature dependence (at the source (T_s), channel (T_{ch}), gate (T_g), and drain (T_d)) on the number of fins, demonstrated for 1, 3, 5, 10, 25, and 50-fin devices. We show the temperatures obtained with (E-Thm) and without (W/O E-Thm) electro-thermal simulations.

L_g	H_g	W_g	H_{fin}	W_{fin}	t_{ox}	L_{ext}	L_q	L_{sd}	W_{sd}
$50nm$	$75nm$	$140nm$	$65nm$	$10nm$	$16\mathring{A}$	$50nm$	$5nm$	$200nm$	$200nm$

H_{sd}	L_{gp}	W_{gp}	W_{space}	R_{if}	k_g	k_{ch}	k_{ext}	k_{ox}	k_{sd}
$65nm$	$200nm$	$200nm$	$100nm$	$20e^{-9}\frac{m^2 \cdot K}{W}$	$45.3\frac{W}{m \cdot K}$	$6.5\frac{W}{m \cdot K}$	$13.0\frac{W}{m \cdot K}$	$1.38\frac{W}{m \cdot K}$	$13.0\frac{W}{m \cdot K}$

TABLE I

MODEL FINFET DIMENSIONS AND THERMAL CONDUCTIVITIES

The peak temperatures of devices with 1, 3, 5, 10, 25, and 50 fins are compared in Figure 9. The results are consistent results with those drawn from Figure 8. Indeed, the maximum temperature at the drain, source, channel, and gate increases with a larger number of fins, but reaches steady state at or beyond 25 fins. For the single-fin device, the source temperature is at a higher temperature than the gate. However, when the device has 3 or more fins, the gate temperature exceeds that of the source. The peak temperature at the drain exhibits the smallest variations across all the examined devices.

2) I_{on} In Multi-Fin Devices: We performed an experiment to validate the need to model the co-dependence of current and heat injection in finFETs. Figure 9 contrasts peak temperatures obtained using electro-thermal simulations against those obtained assuming uniform temperatures for all the fins. In the latter case, we assume the heat injection at each fin is equal to that of a single fin obtained using electro-thermal analysis. In both cases, a $25^{\circ}C$ ambient temperature was assumed. It is clear that ignoring the dependence of the current and thus the heat injection on temperature leads to the gross overestimation of the multi-fin temperature profiles. This is true for all four regions, and worst for the drain ($\sim 20^{\circ}C$).

Figure 8 shows a temperature profile for a 50-fin device. The temperature difference across the fins directly impacts the current through each fin. Using electro-thermal simulations, we examine the current through each fin of a 50-fin device in Figure 10 at different ambient temperatures. As expected, the outer fins carry more current than the inner fins. Equally interesting, the ΔI for the outer vs. inner fins decreases as the ambient temperature increases. This suggests the impact of fin-to-fin interactions diminish at high ambient temperatures.

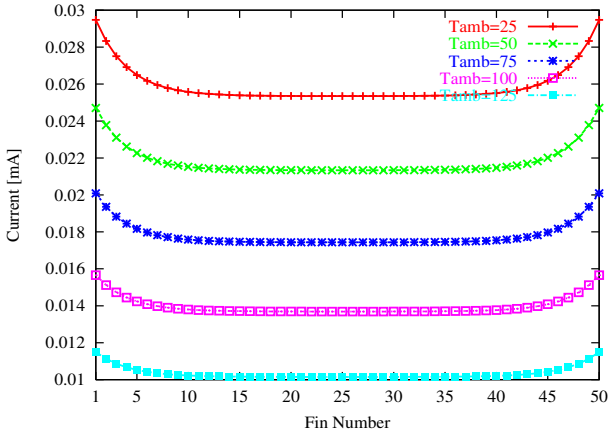


Fig. 10. Current vs. fin number for 50-fin device at different ambient temperatures.

Figure 11 shows the current of multi-fin devices with and without electro-thermal coupling. Electro-thermal coupling uses the individual fin temperature to compute the current through each individual device fin. Currents obtained without electro-thermal coupling assume a uniform temperature (that of a single-fin device) across all fins. The result is lower device temperatures, smaller gradients across the device, and reduced current. The overestimation is less prevalent with fewer fins as the temperature differences across the regions are less acute. The overestimation approaches a constant value for devices with more than 25 fins. From our plot, assuming constant heat injection over predicts current flow through the device by $\sim$15% and $\sim$7% for 50-fin and 10-fin devices respectively.

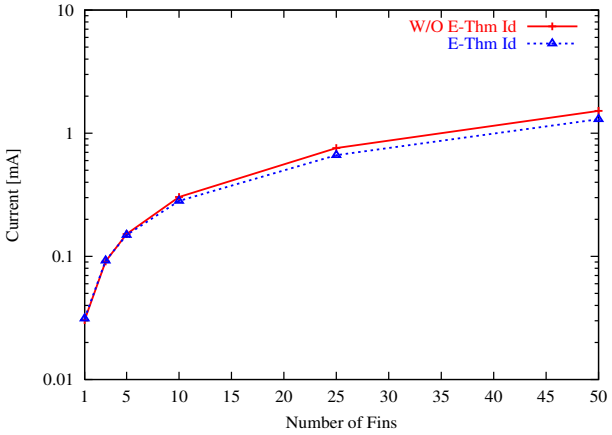


Fig. 11. Current for 1, 3, 5, 10, 25, and 50 fin devices. E-Thm uses electro-thermal simulations, while w/o E-Thm assumes uniform temperatures (that of a single fin obtained via electro-thermal simulation) across all fins.

B. Flared vs. Rectangular Channel Extension Comparison

Flared channel extensions increase I_{on} by decreasing parasitic source/drain resistance. The current increase results in self-heating within the device. This section explores the thermal differences between rectangular and flared channel extensions.

Figure 12 shows two 50-fin device temperature profiles, one with rectangular channel extensions and one with flared channel extensions. The flared channel extension multi-fin thermal model discretized the flared source and drain regions into 100 segments[6]. Several observations can be made when studying Figure 12. First, the maximum device temperature

[6]The electrical model also accounts for the reduced source/drain channel extension resistance by altering the parasitic source/drain resistance.

(T_d) is higher in the flared channel extension device due to a larger I_{on}. Second, the fin-to-fin ΔT is less pronounced in the flared channel extension device. Third, the maximum channel and gate temperatures are relatively close to one another, but deviate significantly at the outer fins. Finally, the source temperature for the flared channel extension is less than the rectangular channel extension source temperature. This can be attributed to the lower source/drain channel extension thermal resistances. The reduced thermal resistances allow more heat to flow out of the drain extension region to the drain pad than into the device. Heat flow which does reach the source regions also has a less restrictive heat flow path to the source pad, thus reducing the source temperature. Flared channel extensions not only reduce source/drain electrical resistance, but also reduce the source-to-pad thermal resistance resulting in a cooler source temperature, thus further increasing I_{on}.

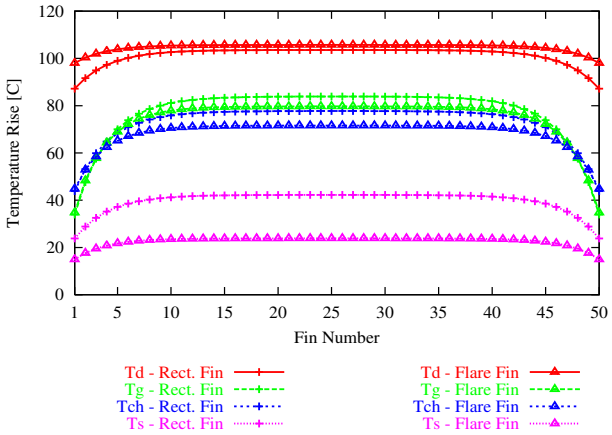


Fig. 12. Temperature profile at the source (T_s), channel (T_{ch}), gate (T_g), and drain (T_d), for a 50-fin device. The rectangular channel extension device is represented by *Rect. Fin*, while the flared channel extension device is shown as *Flare Fin*.

Figure 13 compares maximum device temperatures for the source, channel, gate, and drain regions of rectangular and flared channel extension devices. Complementing the observations made in Figure 9 and Figure 12, one additional conclusion can be drawn from the figure. The drain and source temperatures differences across all device sizes in the flared channel extension devices are less pronounced than in the rectangular channel extension devices, due to the lower thermal resistance of the channel extensions. Less heat flows through the gate poly to the gate pad, reducing the effect of moving the gate pad further away from the inner fins, as shown in Figure 12.

Figure 14 shows the current dependence on the number of fins for rectangular channel extensions and flared channel extensions. Flared channel extensions reduce source/drain parasitic resistance and increase I_{on}, as previously mentioned. Flared channel extensions increase I_{on} over rectangular channel extension devices by ∼1.9x to ∼2.0x for single-fin and 50-fin devices.

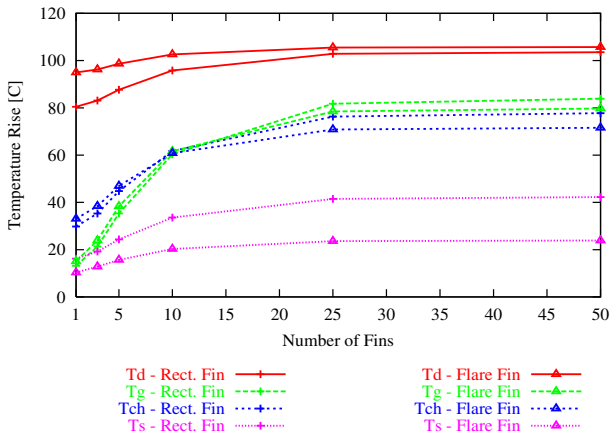


Fig. 13. Temperature dependence (at the source (T_s), channel (T_{ch}), gate (T_g), and drain (T_d)) on the number of fins, demonstrated for 1, 3, 5, 10, 25, and 50-fin devices. The different channel extension configuration are represented as *Rect. Fin* and *Flare Fin*.

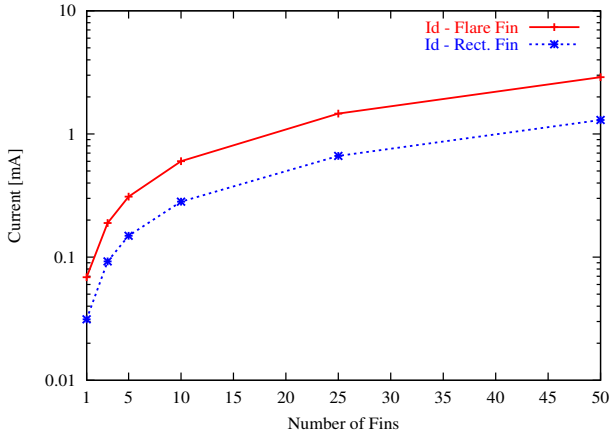


Fig. 14. Current dependence on the number of fins, demonstrated for 1, 3, 5, 10, 25, and 50-fin devices. The different channel extension configurations are represented as *Rect. Fin* and *Flare Fin*.

C. Device Geometries Impact

In our next set of experiments, we quantify the effects of the following parameters, L_g, W_{space}, H_g, T_{ox}, W_{fin}, and H_{fin} on finFET temperature and performance. We vary each parameter as follows. For L_g, we examine several gate lengths between 25nm and 100nm. For fin spacing, W_{space}, we chose 50nm, 100nm, 200nm, and 400nm. For the rest of the parameters we varied them by +/- 10%, and +/- 20% as that would reflect some processing variations.

1) Gate Length Variations: Figure 19(a) and Figure 19(b) plot the maximum drain temperature for multi-fin devices that have 1, 3, 5, 10, 25, and 50 fins, while varying the device length, L_g for rectangular channel extensions and flared channel extensions respectively. Figure 19(a) shows a single-fin temperature difference of ∼5% between the smallest and largest gate lengths for rectangular channel extensions, while Figure 19(b) shows a ∼12% difference for flared channel extensions.

The small temperature variations in the drain are due to

large temperature fluctuations in the source as demonstrated in Figure 21(a) for a rectangular channel extension device. Longer devices typically produce less drive current than shorter devices. However, the thermal resistance between the drain and source is larger in longer devices than in shorter devices. The effect of increased in channel thermal resistance can be inferred from Figure 19(a,b). As the gate length in rectangular channel extensions increases the channel resistance significantly impedes heat flow from the drain to source/gate pads and thus forces all heat to flow out of the drain extension into the drain pad. However, the impact of increased gate length on flared channel extensions is less severe, as the majority of heat flows out of the drain extension into the drain pad as opposed to flowing through the channel to the source/gate pads. The decreased heat flow from drain to source also causes the source to operate at a lower temperature. The lower temperature increases the current in longer devices, whereas higher temperatures degrade the current in shorter devices. This electro-thermal phenomenon is demonstrated in Figure 21(b) for channel lengths of 100nm, 50nm, and 25nm. The difference in current between the 25nm and 100nm devices is $\sim$17% and $\sim$11% for 50-fin and 10-fin devices respectively. Thus, reduced gate lengths do not substantially increase drive current due to the thermal overheads associated with shorter gate lengths.

2) Fin Spacing Variations: We next examine the effect of varying the fin spacing, W_{space}, on the drain temperature. The results are reported in Figure 19(c) for rectangular channel extensions and in Figure 19(d) for flared channel extensions. One would expect that more tightly packed fins to have higher temperatures; however, this is only true for large flared channel extension devices. The tighter spacing reduces R_i between the fins and effectively reduces the gate to pad resistance for each fin. This leads to smaller maximum temperatures as the heat removal path through the gate is less resistive than it is with wider spacing. This indicates that the maximum temperature in each drain is mostly due to electron-phonon interactions rather than heat spreading from neighboring fins. For larger fin spacing, the maximum drain temperature is achieved via few fins: the maximum temperature is almost achieved with a 10-fin device. The important conclusion here is that packing the fins tightly could potentially help with the heat removal. However, the approximation of the heat removal capabilities of the environment (i.e. ignored in this study) is needed to verify this conclusion.

3) Gate Height Variations: In our next experiment, the effect of varying gate height (H_g) on maximum device temperature is quantified. The maximum device temperature vs. number of fins for gate height changes of $\pm$20% nominal is shown in Figure 19(e) for rectangular channel extensions and Figure 19(f) for flared channel extensions. The effect of varying H_g is more evident for devices with a smaller number of fins. Varying H_g has less than a 10% change on the temperatures. Again, this indicates that the heat removal is more prevalent through the source/drain pads than through the gate. This is in support of Pop et al.'s findings that the dimensions of the source and drain are of critical importance [14].

4) Oxide Thickness Variations: We next investigate the impact of oxide thickness variations, T_{ox}, on device temperature and current. The thermal results are shown in Figure 20(a,b) while the electrical results are shown in Figure 22(a,b). Varying T_{ox} by $\pm$20% produces a $\sim$7% change in temperature and a $\sim$6% change in current for the single-fin rectangular channel extension device. Results for the flared channel extension device are more dramatic. Changing T_{ox} by $\pm$20% results in a $\sim$20% change in temperature and a $\sim$15% change in current. The changes in temperature remain relatively constant across different device types and sizes, as shown in Figure 20 (a,b). From a device standpoint, T_{ox} variations have a greater impact on device electrostatics than the device thermal properties. The reason for this is that a) T_{ox} controls the V_T of the device and ultimately effects the current through the device; and b) the thermal conductivity of the oxide (k_{ox}) is much smaller than the other device thermal conductivities (k_g, k_{ch}, k_{ext}, etc.).

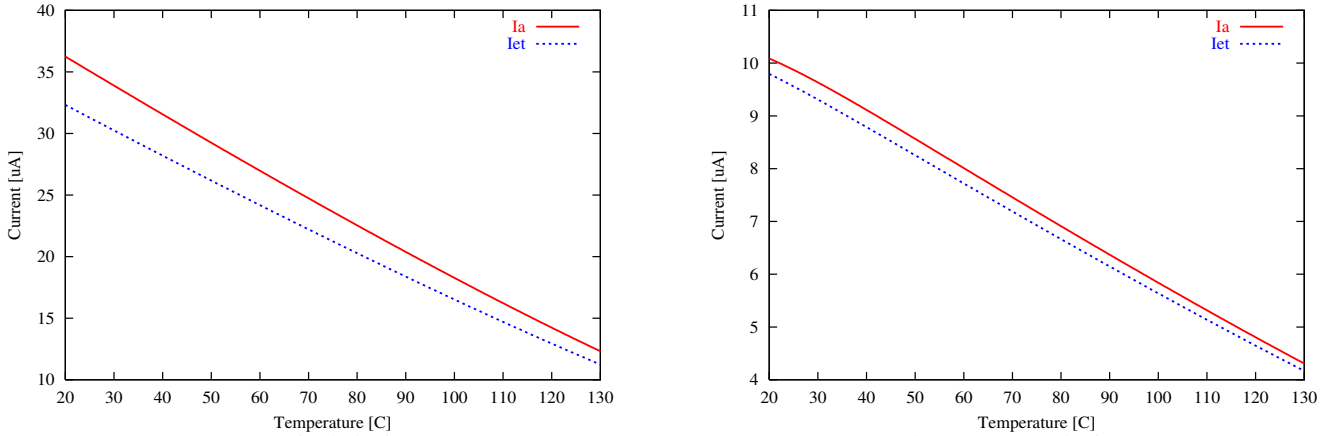
5) Fin Width Variations: Our next experiment examines how W_{fin} affects drain maximum temperature, shown in Figure 20(c) for rectangular channel extensions and Figure 20(d) for flared channel extensions. Changes in fin width affect almost all thermal resistances in the circuit, resulting in significant changes in maximum device temperature for fin width changes of $\pm$20%. Figure 20(c) shows a $\sim$7% difference in maximum temperature for rectangular channel extensions, while Figure 20(d) shows a $\sim$17% difference in temperature for flared channel extensions.

Figure 21(c,d) corroborates these assumptions. In Figure 21(c), a fin width change from nominal of $+$20% lowers the source temperature by $\sim$15% for a 50-fin device. Likewise in Figure 21(d), a fin width change from nominal of $+$20% increases device current for a 50-fin device by $\sim$12%.

6) Fin Height Variations: Our final study examines the impact of H_{fin} on drain temperature and device current as shown in Figure 20(e,f) and in Figure 22(c,d). Increasing H_{fin} ultimately increases the device current as the device width (per fin basis) is defined by H_{fin}. The increase in current results in greater heat generation and higher device temperatures as Figure 20(e,f) shows. Varying H_{fin} by $\pm$20% yields a $\sim$13% change in temperature and a $\sim$45% change in current for a single-fin device with rectangular channel extensions and a $\sim$20% change in temperature with a $\sim$44% change in current for the same device with flared channel extensions. Changing the fin height produces the most variation in temperature among all the other parameters examined. This is because the fin height affects almost all of the thermal resistance values associated with the circuit. A taller fin reduces R_{xs}, R_{xd}, R_{cs}, R_{cd}, and R_{ox}. This in turn reduces the temperature differential between the drain and source regions. The resulting source temperature is reduced, resulting in increased drive current (I_{on}).

D. Thermal Sensitivity of FinFETs

In the previous section, we examined how changes in device parameters affect device temperature and current. All of our comparisons were carried out at a single ambient temperature. In this section, we examine how temperature in conjunction



(a) Nominal device. (b) 0.2x W_{fin} device.

Fig. 15. Current dependence on temperature for single-fin device with rectangular channel extensions. The x-axis temperature represents the ambient temperature.

with variations in device parameters alter device performance. We establish a device *thermal sensitivity* metric and provide insight to the evaluation of device performance in the presence of process and temperature variations.

We begin by looking at a current versus temperature for a nominal single-fin device. Figure 15(a) illustrates the current in the nominal finFET device with and without electro-thermal simulations. I_a is the current obtained assuming the fin is at the ambient temperature (the x-axis in Figure 15(a)). I_{et} is the current obtained using electro-thermal simulations assuming the ambient temperature is the x-axis temperature in Figure 15(a). I_{et} reflects device self-heating as well as the ambient temperature. The figure illustrates the over-estimation of the current without using the electro-thermal simulation. At $20°C$, the difference between the two simulations is $\sim$11%. As the ambient temperature rises it begins the dominant over self-heating and causes the ΔI between I_a and I_{et} to decrease. Thus, the self-heating depends on the ambient temperature. Figure 15(a) also allows the total self-heating to be calculated. At a given current, the difference in temperature between I_a and I_{et} represents the self-heating. For example, a current of $30\mu A$ produces $\sim 17°C$ of self-heating[7].

Geometric parameter variations influence device current and self-heating. Figure 15(b) shows I_a and I_{et} for a finFET with a 0.2x nominal fin thickness. Two observations can be made from the figure. First, the currents, I_a and I_{et}, as well as the difference between the two currents are reduced when compared to the nominal device. Second, the ΔI across all ambient temperatures remains constant, producing *parallel* I_a and I_{et} vs. temperature lines. The parallel lines indicate constant self-heating across all ambient temperatures, resulting in a thermally robust device.

The nominal device in Figure 15(a) is more susceptible to self-heating than the 0.2x nominal W_{fin} device shown in Figure 15(b). Given a set of geometric parameter variations, either process or design, the thermal sensitivity can be calculated to determine robustness to self-heating. Figure 16 shows I_a and I_{et} for fin thickness variations of 0.2x nominal to 2x nominal W_{fin}. As the figures shows, the thermal sensitivity is strongly dependent on the fin thickness variation.

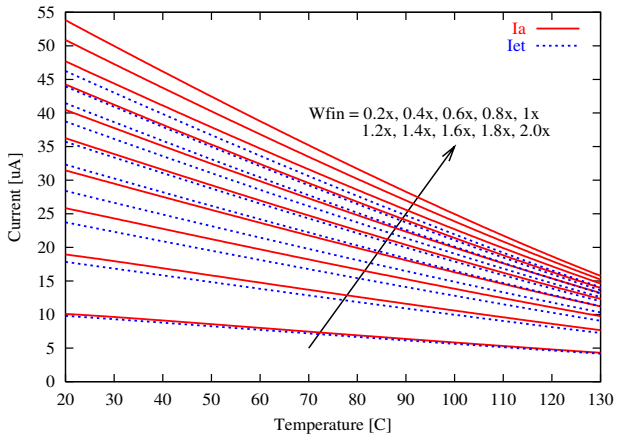


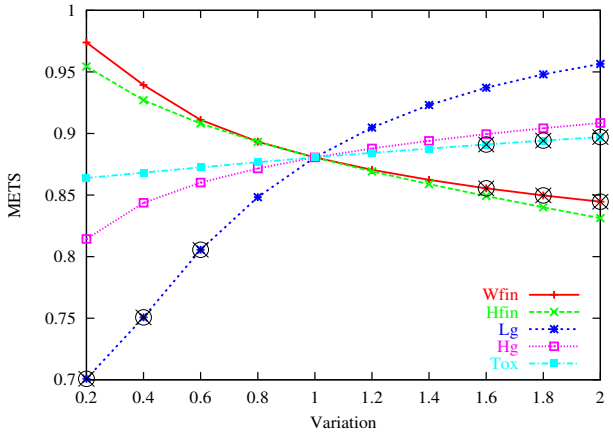
Fig. 16. Current dependence on temperature for single-fin device with rectangular channel extensions for nominal fin thickness variations of 0.2x to 2x.

E. METS: Metric for Electro-Thermal Sensitivity

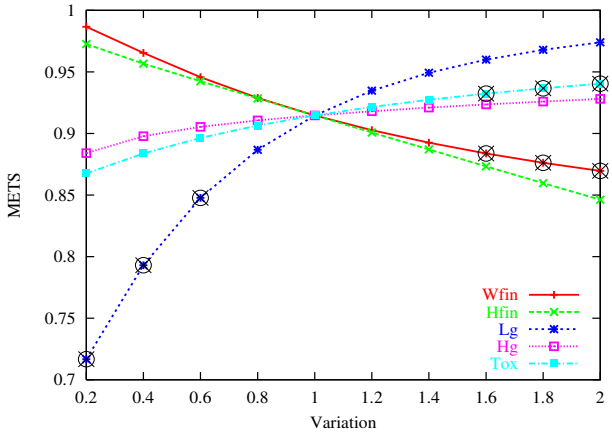
Characterizing thermal sensitivity by I_a and I_{et} becomes infeasible for multiple parameters with large variations due to the enormous amount of data required to evaluate the devices, as demonstrated in Figure 16. Thus, a metric which summarizes the electro-thermal data is required. The metric must have the following characteristics:

- For the metric to be useful, it should not depend on a particular operating temperature. The metric should remove the impact of operating at a particular temperature.
- The metric should be able to capture the effects of device processing and geometries.
- The metric must be independent of the method used to obtain the underlying simulation results as we wish the

[7]All temperatures are in reference to the source temperature, as the source temperature controls carrier injection into the channel and ultimately I_{on} [14], [23].



(a) Rectangular channel extension.



(b) Flared channel extension.

Fig. 17. Thermal sensitivity plot for single-fin devices with rectangular and flared channel extensions. The parameter variations range from 0.2x to 2x, where 1x is the nominal device. The METS range is [0,1] with a value of 1 representing thermal insensitivity. Points with an x through them indicate that the device does not conform to the fin electrical design recommendations.

metric to remain valid with advances in simulation and modeling technologies.

- It is desirable that the metric is general and can be applied to a wide range of devices, thus allowing useful comparisons about device sensitivities in different regions of operation.

Our metric, *METS* (*M*etric for *E*lectro-*T*hermal *S*ensitivity), measures device thermal robustness by summarizing the I_a and I_{et} simulation data [33]. To establish the metric, we utilize the difference between I_a and I_{et} at different temperatures. Each simulation (I_a and I_{et} pair) in Figure 16 is characterized by a sensitivity slope, S_a or S_{et}, over a wide range of operation. The sensitivity slope reflects the change in current due to temperature changes. In the case of S_a, the slope captures changes in ambient temperature. For S_{et}, the slope captures temperature due to both self-heating and ambient temperature. The self-heating metric can be expressed as S_{et}/S_a for each device. *METS* is the computed as:

$$\begin{aligned} METS &= S_{et}/S_a, \text{ where} \\ S_{et} &= \frac{I_{et_{T_2}} - I_{et_{T_1}}}{T_2 - T_1} \\ S_a &= \frac{I_{a_{T_2}} - I_{a_{T_1}}}{T_2 - T_1} \end{aligned} \tag{14}$$

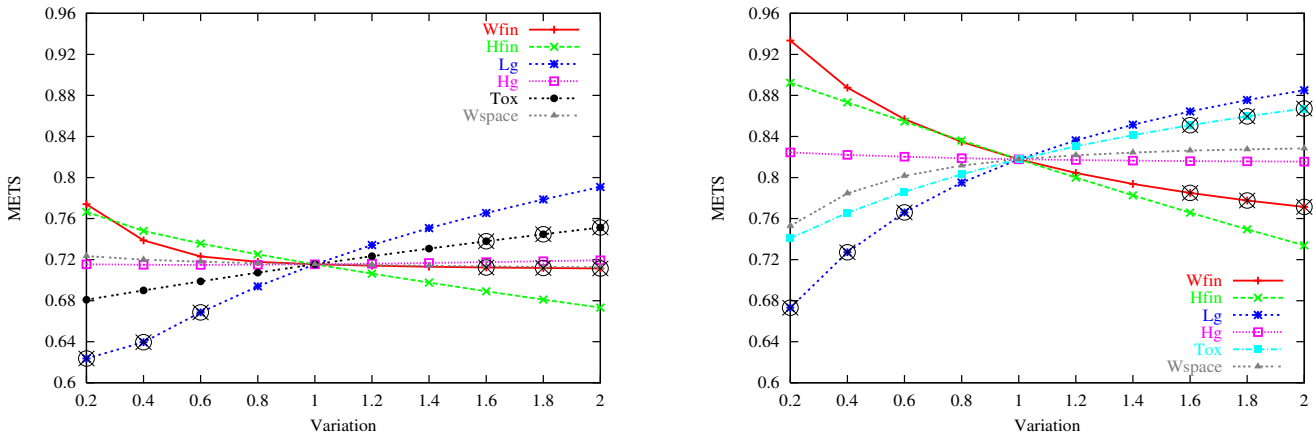
METS is confined to the range of [0,1]. A device with constant self-heating will have *METS* equal to one, that is, I_a and I_{et} will be parallel. However, a device with substantial self-heating will have a *METS* ratio less than one. The temperatures, T_1 and T_2, are selected based on the expected operating range of the device and the I_a/I_{et} relationship. Selecting T_1 and T_2 at the extreme temperatures of the operating region is sufficient for a linear I_a/I_{et} relationship. When the I_a/I_{et} relationship is nonlinear, the operating range can be decomposed into multiple temperature regions and the *METS* can be found for each of the regions. The nominal device shown in Figure 15(a) has a *METS* ratio of 0.88.

Figure 17(a) shows the *METS* ratio for a single-fin rectangular channel extension device with several geometric (W_{fin}, H_{fin}, L_g, H_g, and T_{ox}) variations. The baseline (nominal) device is the single-fin rectangular channel extension device with the parameters shown in Table I. Each point on the graph represents the *METS* for a given deviation from a nominal device, referred to as 1x. Figure 17(b) illustrates the *METS* ratio of a flared channel extension device. For a nominal device, the *METS* ratio of a flared channel extension device is higher than that of a rectangular channel extension device (0.91 vs. 0.88). This indicates that the flared channel extension is effective in reducing the thermal sensitivity of finFETs. The flared channel extension decreases both the thermal and electrical resistance of the extensions resulting in higher device currents and larger heat flow through the extensions to the pads. The geometric variations from the nominal device have less of an impact on both temperature and current thus making the flared device more robust than the rectangular one.

Examining the W_{fin} thermal sensitivity lines in Figure 17(a) and in Figure 17(b) show a thinner fin is more robust than a wider fin. For example, the thermal sensitivity of a 0.2x device is larger than the thermal sensitivity of a nominal device, thus the thinner fin is less sensitive to self-heating. This is justified when comparing the slopes of I_a and I_{et} in Figure 15(b) against the slopes of I_a and I_{et} in Figure 15(a). As Figure 15(b) shows, the slopes are almost parallel resulting in near ideal thermal sensitivity and higher thermal sensitivity than in Figure 15(a).

From the *METS* plots shown in Figure 17, some of the device variations, such as T_{ox} variations, contribute the least to self-heating effects. In contrast, any change in L_g results in significant device self-heating. The circles with X's in them represent devices which do not meet recommended device geometries. For example, Gen *et* al. recommends the ratio: $W_{fin} \leq 0.5\ L_{eff} - 6\ t_{ox}$ for reduced DIBL and ideal subthreshold slope [34]. Yu *et* al. provides the ratio: $W_{fin} \leq 5\ L_{eff}$ for an acceptable fin aspect ratio [7]. The *METS* plot thus provides a good way of evaluating how the device self-heating will change under process variations.

Figure 18(a) shows the *METS* for a 50-fin device with rectangular channel extensions, while Figure 18(b) shows



(a) Rectangular channel extension device.

(b) Flared channel extension device.

Fig. 18. Thermal sensitivity plot for 50-fin devices with rectangular and flared channel extensions. The parameter variation ranges from 0.2x to 2x a nominal device. The METS range is [0,1] with a value of 1 representing thermal insensitivity. Points with an x through them indicate that the device does not conform to the fin electrical design recommendations.

the *METS* for a 50-fin with flared channel extensions. To understand the impact of geometric process variations, W_{fin}, H_{fin}, L_g, H_g, T_{ox}, and W_{space} are varied from 0.2x to 2x, where 1x represents the nominal device (and nominal fin spacing). For each device, the *METS* was calculated according to equation (14). Similar to the single-fin devices, the 50-fin flared channel extension device exhibits higher a *METS* ratio than the rectangular channel extension device (0.81 vs. 0.71). It is also interesting to note the 50-fin devices are more sensitive to thermal variations than the single-fin devices, due to the larger temperature variations within the device. Figure 18(b) shows as the fin spacing is decreased below the nominal fin spacing, the *METS* ratio decreases. This can be attributed to increased heat spreading within the device leading to larger temperature gradients amongst the fins.

The *METS* metric provides a numerical summary of device performance and stability over process and temperature variations. In digital applications, *METS* can be used to predict device stability as different device parameters are varied to meet timing/power/area constraints. In modern digital circuits, the electrical time constant (due to critical path switching speeds) typically dominates over the thermal time constant; thus allowing the use of steady-state temperatures and currents in *METS* calculations. *METS* can also be applied to devices in analog circuits. If a set of device operating points are known, *METS* can be calculated for each of the different regions of operation by adjusting the electrical operating point during the electro-thermal simulation, enabling device stability predictions to the different regions of operation.

VI. Conclusion

We developed in this paper a single-fin flared channel extension thermal model that improves the UTB compact thermal model proposed by Pop *et* al. [14]. We examined several factors that affect the temperatures within multi-fin devices. Fin spacing and gate height contribute to the ability to remove heat effectively away from inner fins to the gate pads. More importantly, the fin width and gate length, contribute significantly to the maximum device temperature. The number of fins clearly affect the maximum temperature where devices with fewer fins exhibit less heating. Tight thermal constraints may require device grouping with a relatively small number of fins in comparison with a large multi-fin device. We have also shown that coupled electro-thermal simulations are needed to accurately capture the electrical and thermal interactions within future nano scale devices. Furthermore, we have presented a thermal sensitivity metric, *METS*,which allows evaluating the temperature sensitivity of a device against device parameter variations.

This work is novel as it is the first to determine the key parameters needed to construct electro-thermally-aware multi-fin devices. Furthermore, our findings motivate further research into the newly emerging area of research, *electro-thermal device design*. There is a need to balance electrical and thermal properties. The impact of confined device geometries and ballistic electron transport on device reliability must be carefully examined. In addition, our device-level thermal study paves the way for circuit or design level thermal investigations. The multi-fin model can be directly utilized in circuit-level SPICE simulation based thermal studies to accurately represent finFET devices in a circuit. Moreover, the coupled electro-thermal simulation demonstrated at the device-level is equally applicable at the circuit-level. Understanding thermal design sensitivities will help understand the impact of device process variations on circuit design, a critical challenge in 45nm and beyond designs.

VII. Acknowledgments

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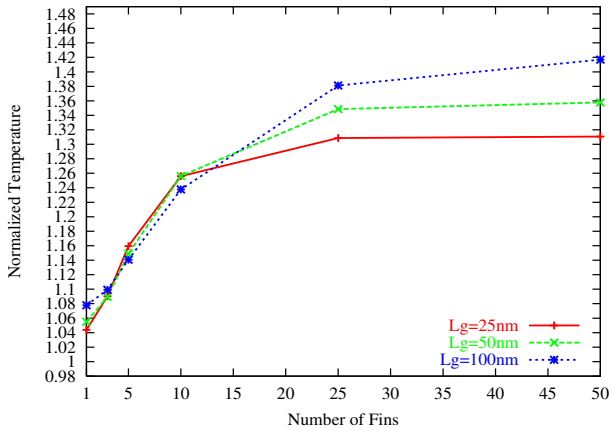
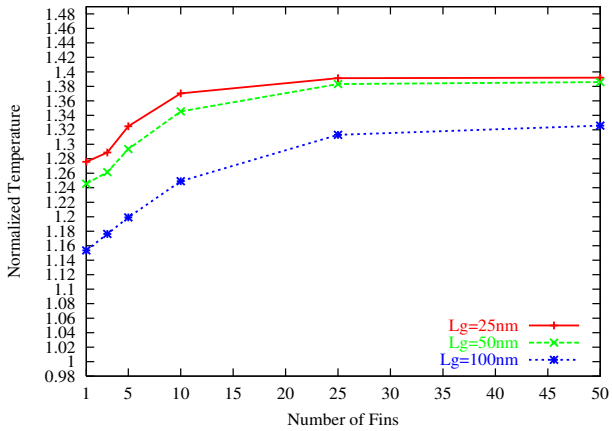
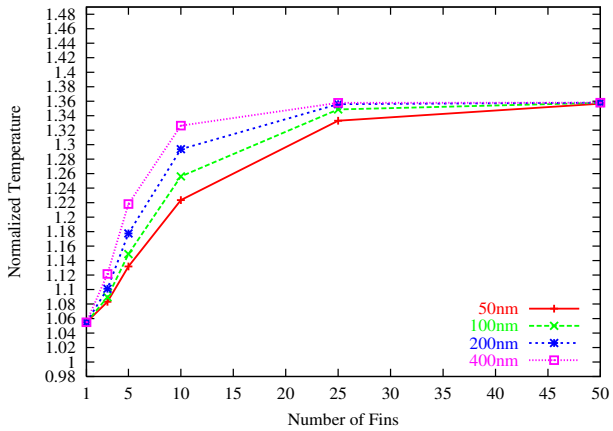


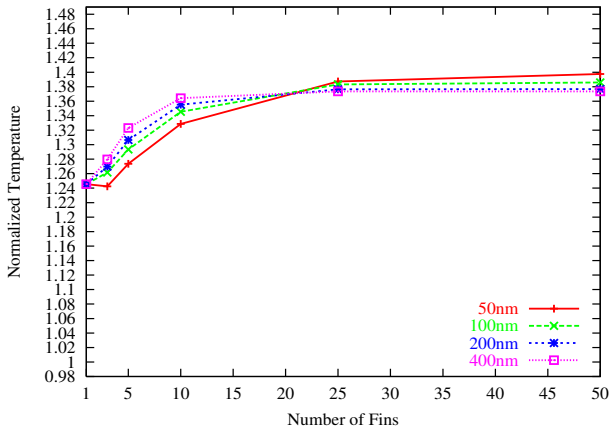
(a) Rect. temperature dependence on L_g.



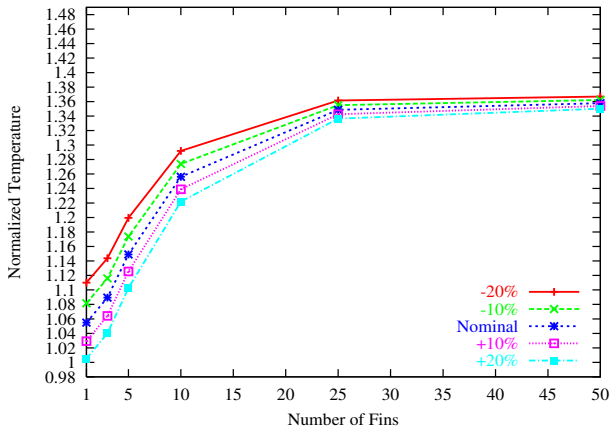
(b) Flared temperature dependence on L_g.



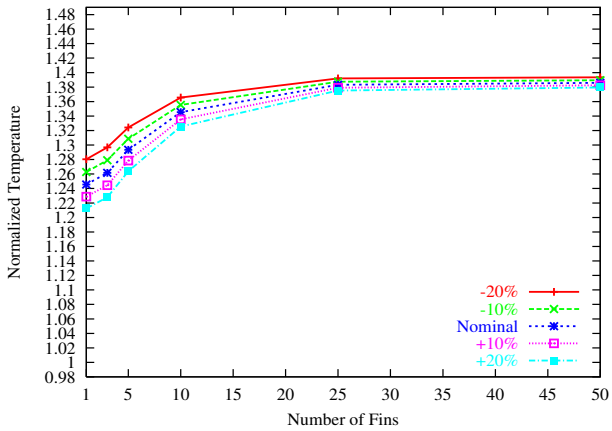
(c) Rect. temperature dependence on W_{space}.



(d) Flared temperature dependence on W_{space}.

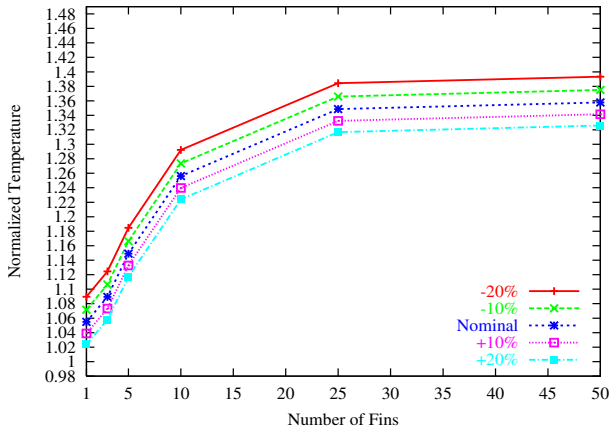


(e) Rect. temperature dependence on H_g.

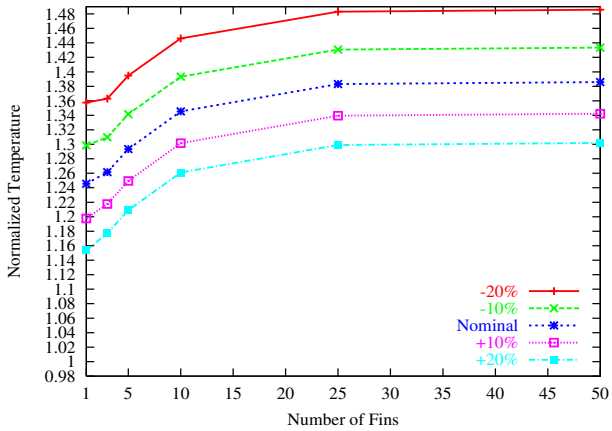


(f) Flared temperature dependence on H_g.

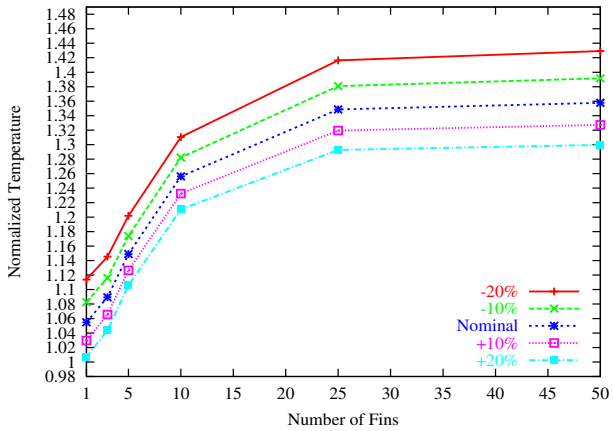
Fig. 19. Experimental data to characterize the effects of different design parameters on maximum device temperature at the **drain** node in rectangular channel extension devices (*Rect.*) and flared channel extension devices.



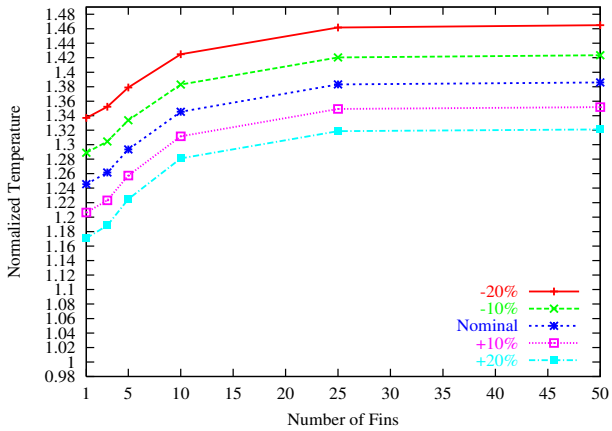
(a) Rect. temperature dependence on T_{ox}.



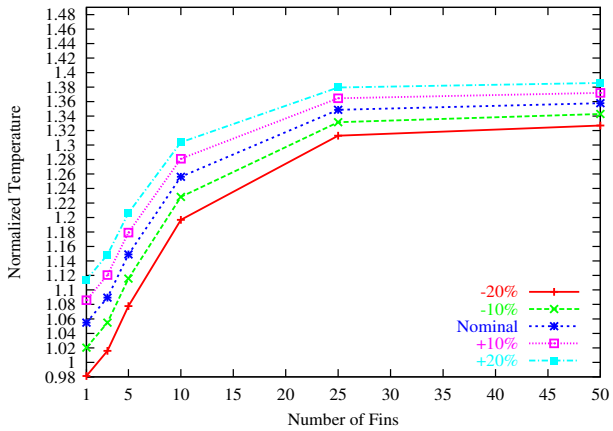
(b) Flared temperature dependence on T_{ox}.



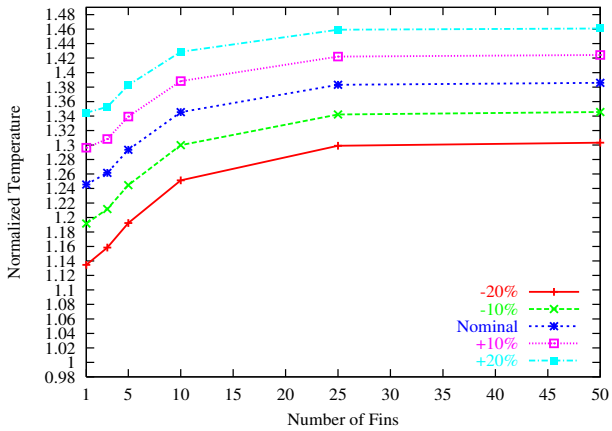
(c) Rect. temperature dependence on W_{fin}.



(d) Flared temperature dependence on W_{fin}.

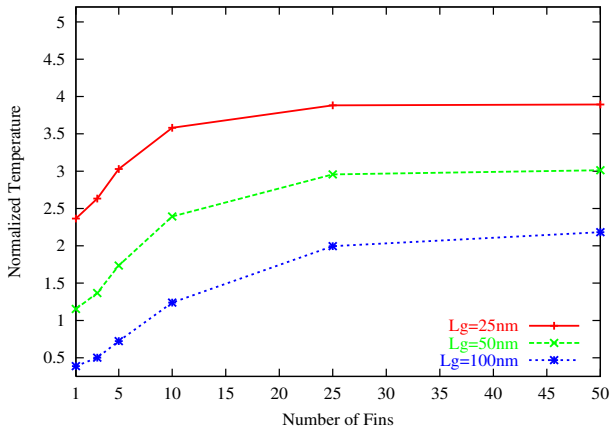


(e) Rect. temperature dependence on H_{fin}.

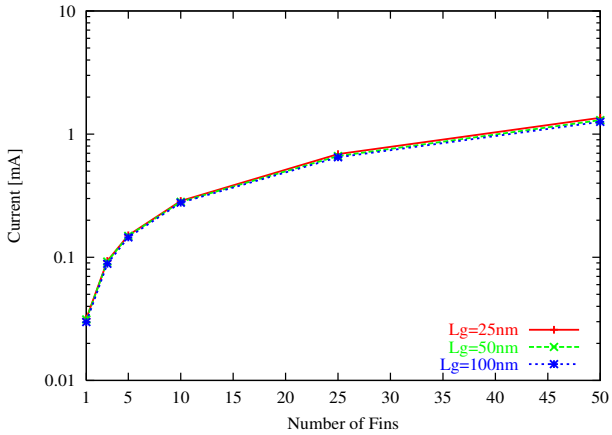


(f) Flared temperature dependence on H_{fin}.

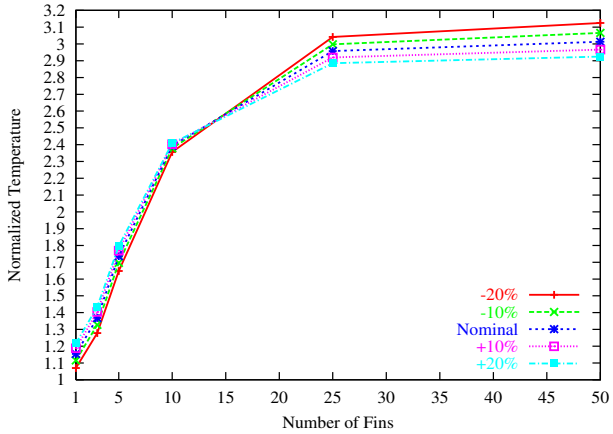
Fig. 20. Experimental data to characterize the effects of different design parameters on maximum device temperature at the **drain** node in rectangular channel extension devices (*Rect.*) and flared channel extension devices.



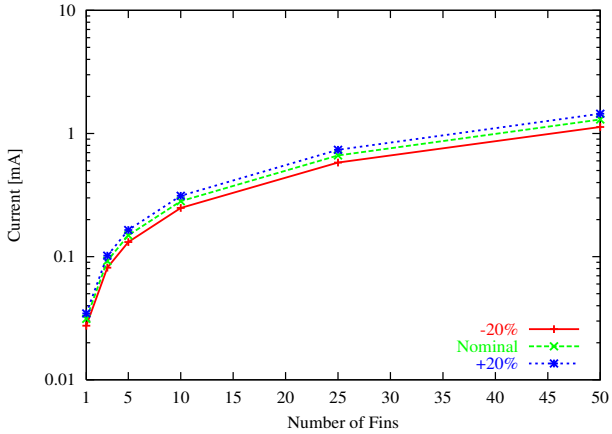
(a) Source temperature dependence on L_g.



(b) Current dependence on L_g.

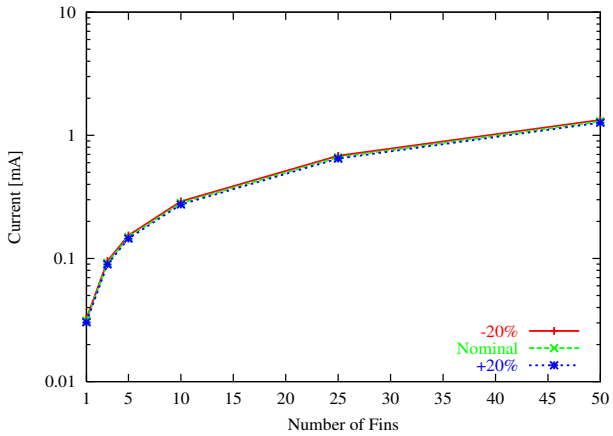


(c) Source temperature dependence on W_{fin}.

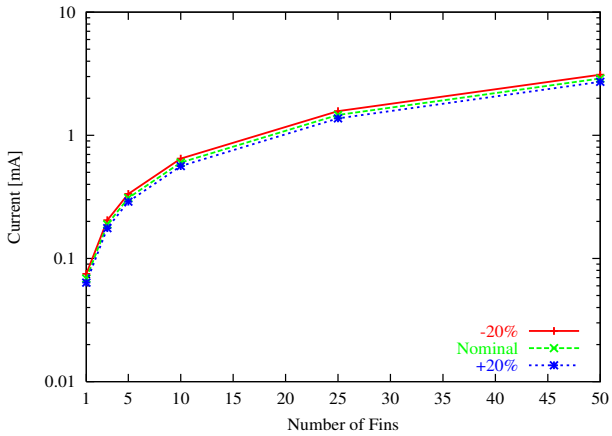


(d) Current dependence on W_{fin}.

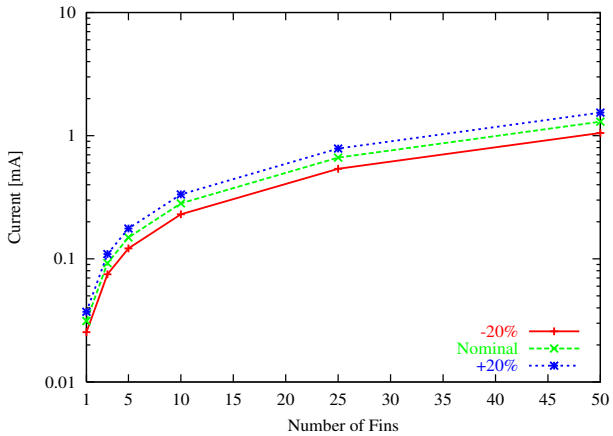
Fig. 21. Source temperature and current dependence on gate length and fin width for rectangular channel extension devices.



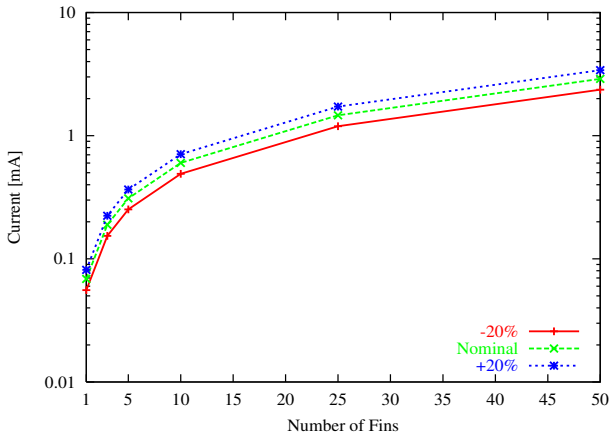
(a) Rect. current dependence on T_{ox}.



(b) Flared current dependence on T_{ox}.



(c) Rect. current dependence on H_{fin}.



(d) Flared current dependence on H_{fin}.

Fig. 22. Current for 1, 3, 5, 10, 25, and 50 fin devices for different oxide thicknesses and fin heights in rectangular channel extension devices (*Rect.*) and flared channel extension devices.