JOEL GRODSTEIN
Curriculum Vitae

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Research interests

- VLSI design
- Computer-aided design and validation tools for integrated circuits
- Optimization problems, especially in the Boolean and mixed algebraic-Boolean domains, applied to both the above areas.
- Synthetic biology, systems biology and biological physics, especially as they relate to computing and optimization.

Honors and Awards

- IEEE Transactions on CAD Best Paper, 1999, for logic synthesis. One of the rare times this award has gone to a team not from a university or an industrial research group.
- IEEE ICCAD, inclusion in a special-edition book, "The Best of ICCAD," for one of the 8 best papers on logic synthesis in 20 years.

Career highlights

- Technical leadership positions on numerous microprocessor designs, CAD projects and post-silicon debug teams.
- Deep expertise in VLSI post-silicon debug, test, circuit design, DFX architecture, static timing, logic synthesis and noise analysis from both a theoretical and a practical point of view.
- Led the logic-synthesis team that developed gain-based mapping graphs for technology mapping. This became standard material in college logic-synthesis courses, helped lead to the launch of a new company (Magma Design Automation), and won several professional honors (see below).
- Led the development of arguably the first industrial-strength transistor-level static timing analyzer.

Education

- University of Utah, MS, Computer Science, 1986
- Case Western Reserve University, BS, Electrical Engineering, 1981
- Coursework at Tufts in 2016/2017 in Biological Physics, Biomedical Transducers, Metabolic Engineering and Bioinformatics, and Synthetic Biology.

Professional experience

Lecturer, Tufts University

- 2016-present. Taught multiple courses in VLSI design, computer architecture, parallel computing and bioelectricity

Principal Engineer, Intel

- *2014: DFX architect*. Was the representative of tester-debug for all DFX architecture and implementation concerns for all Intel products.
- *2013-14: Memory DFX architect*. Defined the memory-test architecture and tooling for all Intel servers.

- *2005-13: Tester debug.* Technical lead of a tester-debug team that owned all electrical debug, including clock-speed improvement, over multiple CPU generations of Itanium and Xeon servers.
- *2003-5: Test/debug Implementation Leader.* Led implementation of all test and debug features on Intel's Tukwila Itanium processor.

Principal Engineer, Compaq and HP

- *2001-2: Path-delay ATPG project leader*. Responsible for defining and implementing a CAD tool to automatically generate scan-based tests for critical paths.
- *1998-01: Alpha 21364 CPU*. Dual CAD/design role. Responsible for CAD & methodology decisions & work scheduling for a team of 40 CAD engineers. Also responsible for design and verification of a 1.1 Ghz, 1.75 Mbyte L2 cache.

Consulting engineer, Digital Equipment Corporation

- *1996-98: StrongArm 1500*. Served as the project's lead architect for computer graphics. Also did all implementation & microarchitecture for the Load/Store Unit, and all microarchitecture for the instruction/pipeline sequencer unit.
- *1995-96: CAD liaison.* Served as the liaison for the StrongARM 110 CPU. Coordinated all CAD requests, jointly set priorities and schedules. Responsible for ultimate delivery of all CAD work to the CPU team. Also had individual responsibility for the static race-analysis tool.
- *1991-93: Logic Synthesis Project leader.* Led a team of four engineers delivering a next-generation logic-synthesis tool. The tool was delivered on time, and generated circuits that were on average 30% faster than those from Synopsys Design Compiler.
- *1989-91: Static Timing Verification Project Leader.* Led the development of transistor-level static-timing-analysis tools for critical paths and races. These were arguably the first static timing verifiers successful in a full-custom, transistor-level design environment. They were used by three generations of Alpha CPUs.
- *1988-89: Floating-point chip design*. Worked on a team of three engineers shrinking a floating-point chip to a smaller, faster CMOS process.
- *1986-88: numerical analysis***.** Worked on a version of Spice. Added enhancements, including a mixed logic-circuit capability.

Hardware design engineer, Evans & Sutherland Computer Corp.

- *1983*: Designed a 200-chip subsystem for a high-performance computer-graphics workstation.
- *1981-2*: Participated in the design of a custom IC for a graphics pipeline.

Publications (not including Intel-internal publications)

1. Stability and Robustness Properties of Bioelectric Networks: A Computational Approach, J.Grodstein and M.Levin, Biophysics Rev. 2, Sept 2021
2. A Fast Boolean Solver for choosing load/store addresses to test a CPU uncore, J. Grodstein et. al., North Atlantic Test Workshop 2011
3. Test Vector Generation for Post-Silicon Delay Testing using SAT-Based Decision Problems, D. Tadesse, R.I. Bahar, J. Grodstein, Journal of Electric Testing, April 2011.
4. AutoRex: An automated post-silicon clock tuning tool, D. Tadesse, J. Grodstein, R.I. Bahar, 2009 International Test Conference

5. Fast Measurement of the "Non-deterministic Zone" in Microprocessor Debug using Maximum Likelihood Estimation, D. Tadesse, R. I. Bahar, J. Grodstein, VLSI Test Symposium 2008
6. Accurate Timing Analysis using SAT and Pattern-Dependent Delay Models, D. Tadesse, D. Sheffield, E. Lenge, R. I. Bahar, J. Grodstein, DATE 07
7. Timing Analysis for Full-Custom Circuits Using Symbolic DC Formulations, R.Iris Bahar, Hui-Yuan Song, Kundan Nepal, Joel Grodstein. IEEE T.CAD. Dec 2006.
8. Accurate Timing Analysis using SAT and Pattern-Dependent Delay Models, Desta Tadesse, Michael Black, Iris Bahar, Joel Grodstein.. ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU), 2006.
9. Symbolic Failure Analysis of Complex CMOS Circuits Due to Excessive Leakage Current and Charge Sharing, R.Iris Bahar, Hui-Yuan Song, Kundan Nepal,Joel Grodstein, IEEE T.CAD., V.24#4, Apr 2005
10. RESTA: A Robust, Extendable Symbolic Timing Analysis Tool, K.Nepal, H.Y.Song, R.I.Bahar, J.Grodstein, GLSVLSI 2004 Poster.
11. Automatic Generation of Critical-Path Tests for a Partial-Scan Microprocessor, J.Grodstein,D.Bhavsar,V.Bettada,R.Davies, ICCD ’03.
12. Symbolic Failure Analysis of Custom Circuits Due to Excessive Leakage Current, H.Y.Song,S.Bohidar,R.I.Bahar,J.Grodstein, ICCD’03.
13. Timing Analysis for Full-Custom Circuits Using Symbolic DC Formulations, H.Y.Song,R.I.Bahar,J.Grodstein, IWLS’02.
14. Power and CAD Considerations for the 1.75 Mbyte, 1.2GHz L2 cache of the Alpha 21364 Microprocessor, J.Grodstein et.al., Great Lakes Symp. on VLSI, April ’02.
15. An ADD-Based Symbolic Analysis of Leakage Current in CMOS Circuits, H.Y.Song,R.I.Bahar,J.Grodstein, IWLS’01 poster.
16. A 1.2GHz Alpha Microprocessor with 44.8GB/s Chip Pin Bandwidth, A.Jain, J.Grodstein, et.al.,ISSCC ’01.
17. Static Race Verification for Networks with Reconvergent Clocks, J. Grodstein et.al., ICCD ’98
18. A Low-Cost 300 Mhz RISC CPU with Attached Media Processor, S.Santhanam, J.Grodstein,et.al.,ISSCC ’98 & in IEEE J. Solid State Circuits, Vol 33, #11, Nov. ‘98
19. Logic Decomposition During Technology Mapping, E.Lehman,Y.Watanabe,J.Grodstein,et.al., IEEE Trans. CAD, Aug 1997
20. A Delay Model for Logic Synthesis of Continuously-Sized Networks, J. Grodstein et. al., ICCAD '95
21. Logic Decomposition During Technology Mapping, E. Lehman, Y. Watanabe, J. Grodstein, et. al.,ICCAD '95
22. Optimal Latch Mapping and Retiming Within a Tree, J. Grodstein et. al., ICCAD '94.
23. A Simple Algorithm for Fanout Optimization using High-Performance Buffer Libraries, Kodandapani, Grodstein, et. al., ICCAD '93
24. Timing Verification on a 1.2M-Device Full-Custom CMOS Design, J.Pan, J.Grodstein et al, DAC 1991
25. Automatic Detection of MOS Synchronizers for Timing Verification, J. Grodstein et. al., ICCAD '91
26. Race Detection for Two-Phase Systems, J. Grodstein et. al., ICCAD '90
27. Constraint Identification for Timing Verification, J. Grodstein et. al., ICCAD '90

28. System, Process, and Design Implications of a reduced-supply-voltage microprocessor, R.Allmon, J.Grodstein, et.al., ISSCC ’90.
29. Spice-Decsim Interface, J. Grodstein et. al., Colorado Microelectronics Conference, 1989.
30. Sisyphus – An Environment for Simulation, J. Grodstein et. al., ICCAD '87

Invited talks

1. Invited Speaker, U.C. Berkeley CAD seminar, 1998, talking about CAD challenges of high-speed chip design.

Patents

1. Timing Verification Using Synchronizers And Timing Constraints, U.S. Patent #5657239, 8/12/97
2. Static timing verification, U.S. Patent #5355321, 11/11/94.
3. Static timing verification in the presence of logically false paths, U.S. Patent #5648909, 7/15/1997
4. Pruning of short paths in static timing verifier, U.S. Patent #6046984, 4/4/2000
5. Method of minimizing area for fanout chains in high-speed networks, U.S. Patent #5648911, 7/15/1997
6. Implicit tree-mapping technique, U.S. Patent #5801957, 9/1/98
7. Method and system for absorbing defects in high performance microprocessor with a large n-way set associative cache, U.S. Patent #6671822, 12/30/03.
8. Latch that Uses a Different Clock for “1” than for “0” Data, IP.com disclosure #IPCOM000128959D, 9/22/2005

Professional service

1. Technical Program Committee, Neuromorphic and Biological Systems Track, ICCAD, 2018
2. Expert Reviewer, ICCAD, 2017
3. Technical Program Committee, VLSI Design track, Great Lakes Symposium on VLSI, 2011
4. Track Co-chair, Tools and Methodology, ICCD 1999
5. Reviewer, IEEE Transactions on CAD, several papers

Teaching

- Bioelectricity (twice)
- Advanced Computer Architecture, Tufts Comp140/EE194, Spring 2016 (Co-taught)
- Introduction to Computational Design, Tufts EN01-4, Fall 2016
- Computer-Aided Design for VLSI, Tufts COMP150-CAD, Spring 2017
- Parallel Computation, three times
- Advanced VLSI Design, Spring 2018
- Modeling, simulating and optimizing biological systems, twice
- Synthetic Biology, Tufts CHBE193/EE193, Fall 2018 (co-taught twice)
- Computer Engineering, EE126, Fall 2018 (twice)

Supervised PhD theses (as industrial-liaison committee member)

- Desta Tadesse, Mathematical Methods to Improve Post-Silicon Debug, 2009

- Hui-Yuan Song, Symbolic Methods for Reliability and Timing Analysis for Full-custom Circuits, 2005

Classes taken at Tufts

- BIO 196 (Neuromechanics of Locomotion), Spring 2017
- COMP 150 (Current Challenges in Computational Biology), Fall 2016
- CHBE 167 (Metabolic and Cellular Engineering), Fall 2016
- BIO 119 (Biophysics), Spring 2016
- BME 100 (Design of Medical Instrumentation), Spring 2016