COMP 103, Fall 2003  
Homework #5, Due: Tuesday, October 7, 2003

Reading assignments that cover last week’s lectures:
Layout & Design Rules: Chapter 2, (sections 2.3; appendix A)
MOS Capacitance: p. 81-82, p. 110-112, 194-199
MOS resistance: p. 104-106, 113,
Wire Capacitance & Resistance: Chapter 4: sections 1, 2, 3 (through p. 159).

No detailed calculations were required for this homework – but do study all equations presented in the last two lectures carefully. It is more important to know that doubling xd doubles the overlap capacitance than plugging in the numbers.

Problem #1 – Layout

Draw the equivalent transistor circuit for the given layout. What function does this layout implement? What style of logic?

![Diagram of transistor layout](image)
Problem #2 – Parasitic Capacitances of a NAND gate

Consider a NAND gates with two inputs: A & B, shown below. We wish to determine the equivalent RC trees under different operating conditions.

You will be spared the agony of calculating the areas and the capacitances from an actual layout, so use parasitic capacitance symbols in your answer. For example, $C_{DB1}$ will refer to the drain-bulk diffusion capacitance of transistor M1. Don’t forget to account for the Miller Capacitance where appropriate.

For each of the two cases below
1. *draw* the equivalent RC charging or discharging networks, and
2. *write* the expression for the capacitance at nodes out and z.
3. *write* the expression for the LUMPED RC delay at output node, and
4. *write* the expression for the Elmore delay at the output node based on considering the circuit as a distributed RC network.

   a) Assume that input A = VDD and B switches from VDD to Gnd. Both Out and Z will rise.

   b) Assume that input B = VDD and A switches from VDD to Gnd.

   c) How do the delays compare to each other using the lumped v.s. Elmore delays?
**Problem #3 – CMOS Logic**

a. Do the following two circuits below implement the same logic function? If yes, what is that logic function? If no, give Boolean expressions for both circuits.

b. Will these two circuits’ output resistances always be equal to each other? (since Ron is much bigger than parasitic src/drain resistance, ignore the latter)

c. Will these two circuits’ rise and fall times always be equal to each other? Why or why not?
**Problem #4 – Wire Resistance & Capacitance**

We will soon learn that clock distribution networks are critical to performance.

The figure below shows a clock-distribution network. Each segment of the clock network (between the nodes) is 5 mm long, 3 µm wide, and is implemented in polysilicon. At each of the terminal nodes (such as \( R \)) resides a load capacitance of 100 fF.

**a.** Determine the average current of the clock driver, given a voltage swing on the clock lines of 5 V and a maximum delay of 5 nsec between clock source and destination node \( R \). For this part, you may ignore the resistance and inductance of the network. Think basic definitions of current!

**b.** Unfortunately the resistance of the polysilicon cannot be ignored. Draw the equivalent RC network and annotate the values of resistors and capacitors.

**c.** Determine the Elmore delay dominant time-constant of the clock response at node \( R \).