To prepare for this homework, read through the lecture notes and textbook about dynamic logic and timing. To become good at analyzing how latches work, you must spend the time to study them in detail.

**Problem #1: Designing Dynamic Circuits**
Detecting that the value of a bundled signal (or a bus) is zero is very important in processor design. Design an 8-input dynamic circuit that performs a zero detect on signal IN[7:0]. You can use at most 10 transistors. The circuit’s output will precharge to Vdd when the clock is low, and remain charged to one if all inputs are low. If any of the inputs is high, then the output will pull low.

**Problem #2: Dynamic Adder**

This circuit implements a 1-bit datapath function in dynamic logic.

a. Write the boolean expression for output F.
b. Write the boolean expression for output G.
c. On which clock phases is output F valid?
d. On which clock phases is output G valid?
e. When are the inputs (A, B, Cin) allowed to change so that the circuit works properly? Explain your answer.
f. What is the purpose of transistor M1?
g. How can be evaluation phase of F be sped up by rearranging transistors? (no transistors should be added, deleted or resized)
h. Can evaluation of G be sped up by rearranging transistors? Explain your answer.
Problem #3 -- Charge Sharing

For this problem, please assume the following:

The bulk of your transistors are tied to their respective supplies

\( C_{db,p} = C_{sb,p} = C_{db,n} = C_{sb,n} = 10.0\, \text{fF} \)

\( C_{gd,p} = C_{gd,n} = 15.0\, \text{fF} \)

\( V_{tp} = 1.0\, \text{V} \)

\( V_{dd} = 5.0\, \text{V} \)

Your circuit is shown below. !VDD refers to global VDD lines, and !GND refers to global GND lines (notation common in many methodologies) Node X is between the two transistors in series and Node Y is directly under the PMOS device clocked with Clk.

---

a) What is the logic function of the above circuit?
b) What are the capacitances at nodes x, y, and out?

\[ C_x = \]

\[ C_y = \]

\[ C_{out} = \]
c) Given the following inputs, shown in Figure 1b, please trace out the waveforms at the following nodes: \( X \), \( Y \), and \( OUT \). Assume that these nodes are initially at ground.

Approximate the **timing**, but be **accurate** when indicating the voltage levels for the waveforms. *Be sure to show your work.*
Problem #4: Sequential Circuits

The following latch was used on the Power PC. Draw the waveforms for nodes M and Q. ASSUME that M is initially HIGH, and that Q is initially LOW.
PROBLEM #5: Combining Latches and Dynamic Logic

Consider the following circuit (implemented in the 1.2 µm CMOS technology). Assume $V_{DD} = 3$ V.

![Circuit Diagram]

**a.** Fill in the missing clock connections on the schematics (marked by the gray boxes) so that the circuit will operate correctly. For each connection you can choose between $\phi$ and $!\phi$. You may assume here that they are non-overlapping and that there is no skew.

**b.** The circuit cascades a number of dynamic and static logic stages. Assuming no clock overlap, will the proposed configuration evaluate correctly? Explain why or why not.

**c.** Is the circuit sensitive to clock overlaps between $\phi$ and $!\phi$. Explain your answer.

**d.** If the logic between the two latches is replaced with static logic, will the circuit still be sensitive to clock overlaps between $\phi$ and $!\phi$. Explain your answer.

[clock skew was not covered in class, but I expect that you learned enough fundamentals about dynamic circuit operation and latching that you can answer these two questions!]

**e.** Assume that the output latch is located at a very remote site on the chip, and it gets clocked $\delta$ psec after the input latch and evaluation logic is clocked. Is the circuit sensitive to clock skew in this case (either during evaluation or precharge) ? Explain your answer.

**f.** Assume that the output latch is located at a very remote site on the chip, and it gets clocked $\delta$ psec before the input latch and evaluation logic is clocked. Is the circuit sensitive to clock skew in this case (either during evaluation or precharge) ? Explain your answer.