MOS – Long Channel Equations

- When $V_{GS} > V_T$, MOS is ON

- Linear: When $V_{DS}$ is small: $V_{DS} \leq V_{GS} - V_T$
  $$I_D = \frac{k_n}{V_T} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - V_{DS}^2/2\right]$$

- When $V_{DS}$ is large: $V_D \geq V_{GS} - V_T$
  $$I_D' = \frac{k_n}{2} \frac{W}{L} \left[(V_{GS} - V_T)^2\right]$$

- Linear or quadratic dependence on $V_{GS}$
Long Channel I-V Plot (NMOS)

NMOS transistor, 0.25um, $L_d = 10\mu m$, $W/L = 1.5$, $V_{DD} = 2.5V$, $V_T = 0.4V$

Short Channel Effects

- Behavior of short channel device mainly due to
  - **Velocity saturation**
    - the velocity of the carriers saturates due to scattering (collisions suffered by the carriers)

- For an NMOS device with L of .25μm, only a couple of volts difference between D and S are needed to reach velocity saturation
**Voltage-Current Relation: Velocity Saturation**

For short channel devices

- **Linear:** When \( V_{DS} \leq V_{GS} - V_T \)
  \[
  I_D = \kappa(V_{DS}) \ k' W/L [(V_{GS} - V_T)V_{DS} - V_{DS}^2/2]
  \]
  where
  \[
  \kappa(V) = \frac{1}{1 + (V/\xi_c L)}
  \]
  is a measure of the degree of velocity saturation
  
  For large \( L \) or small \( V_{DS} \), \( \kappa \) approaches 1.

- **Saturation:** When \( V_{DS} = V_{DSAT} \geq V_{GS} - V_T \)
  \[
  I_{DSat} = \kappa(V_{DSAT}) \ k' W/L [(V_{GS} - V_T)V_{DSAT} - V_{DSAT}^2/2]
  \]

**Velocity Saturation Effects**

For short channel devices and large enough \( V_{GS} - V_T \)

- \( V_{DSAT} < V_{GS} - V_T \) so the device enters saturation before \( V_{DS} \) reaches \( V_{GS} - V_T \) and operates more often in saturation

- \( I_{DSAT} \) has a linear dependence wrt \( V_{GS} \) so a reduced amount of current is delivered for a given control voltage
Short Channel I-V Plot (NMOS)

NMOS transistor, 0.25um, $L_d = 0.25\,\mu m$, $W/L = 1.5$, $V_{DD} = 2.5V$, $V_T = 0.4V$

MOS $I_D$-$V_{GS}$ Characteristics

- Linear (short-channel) versus quadratic (long-channel) dependence of $I_D$ on $V_{GS}$ in saturation
- Velocity-saturation causes the short-channel device to saturate at substantially smaller values of $V_{DS}$ resulting in a substantial drop in current drive

(for $V_{DS} = 2.5V$, $W/L = 1.5$)
**Short Channel I-V Plot (PMOS)**

- All polarities of all voltages and currents are reversed

![Short Channel I-V Plot](image_url)

PMOS transistor, 0.25um, Ld = 0.25um, W/L = 1.5, VDD = 2.5V, V_T = -0.4V

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**The MOS Current-Source Model**

- ID = 0 for V_{GS} - V_T ≤ 0
- ID = k’ W/L [(V_{GS} - V_T)V_{min} - V_{min}^2/2](1+λV_{DS}) for V_{GS} - V_T > 0

with V_{min} = min(V_{GS} - V_T, V_{DS}, V_{DSAT})

- Determined by the voltages at the four terminals and a set of five device parameters

<table>
<thead>
<tr>
<th></th>
<th>V_T(V)</th>
<th>γ(V^{0.5})</th>
<th>V_{DSAT}(V)</th>
<th>k’(A/V^2)</th>
<th>λ(V^{-1})</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>0.43</td>
<td>0.4</td>
<td>0.63</td>
<td>115 x 10^{-6}</td>
<td>0.06</td>
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<tr>
<td>PMOS</td>
<td>-0.4</td>
<td>-0.4</td>
<td>-1</td>
<td>-30 x 10^{-6}</td>
<td>-0.1</td>
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</table>
The Transistor Modeled as a Switch

Modeled as a switch with infinite off resistance and a finite on resistance, $R_{on}$

- Resistance inversely proportional to $W/L$ (doubling $W$ halves $R_{on}$)
- For $V_{DD} >> V_T + V_{DSAT}/2$, $R_{on}$ independent of $V_{DD}$
- Once $V_{DD}$ approaches $V_T$, $R_{on}$ increases dramatically

<table>
<thead>
<tr>
<th>$V_{DD}$ (V)</th>
<th>1</th>
<th>1.5</th>
<th>2</th>
<th>2.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS (kΩ)</td>
<td>35</td>
<td>19</td>
<td>15</td>
<td>13</td>
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<tr>
<td>PMOS (kΩ)</td>
<td>115</td>
<td>55</td>
<td>38</td>
<td>31</td>
</tr>
</tbody>
</table>

R_{on} (for W/L = 1)

For larger devices divide $R_{eq}$ by W/L

Other (Submicon) MOS Transistor Concerns

- Velocity saturation
- Subthreshold conduction
  - Transistor is already partially conducting for voltages below $V_T$
- Threshold variations
  - In long-channel devices, the threshold is a function of the length (for low $V_{DS}$)
  - In short-channel devices, there is a drain-induced threshold barrier lowering at the upper end of the $V_{DS}$ range (for low $L$)
Subthreshold Conductance

- Transition from ON to OFF is gradual (decays exponentially)
- Current roll-off (slope factor) is also affected by increase in temperature
- Has repercussions in dynamic circuits and for power consumption

Threshold Variations

- Threshold as a function of the length (for low $V_{DS}$)
- Drain-induced barrier lowering (for low $L$)
Scaling Analysis

- Manufacturing allows constant reduction in transistor channel length
- A reduction of 13% per year, halving every 5 years.
- Scaling analysis: how reduction in feature size influences the operating characteristics and properties of MOS transistors

Three different models are assume:
  - Full Scaling: everything scales by 1/S
  - Fixed-Voltage scaling: everything scales by 1/S except voltages (supply voltage, threshold voltage)
    - Integration issues: 5V was standard, and now 3.3V and 2.5V
    - Silicon bandgap and built-in junction potentials are material parameters
    - Scaling Vt is limited: can’t turn device 100% off – Bad Leakage problems
    - No more benefits for shorter transistors
  - General Scaling:
    - Device features scale by 1/S
    - Voltages scale by 1/U

Scaling Examples

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Relation</th>
<th>Full Scaling</th>
<th>General Scaling</th>
<th>Fixed-voltage scaling</th>
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<tbody>
<tr>
<td>W, L, tox</td>
<td>1/S</td>
<td>1/S</td>
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<td>1/S</td>
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<tr>
<td>Vdd, Vt</td>
<td>1/S</td>
<td>1/U</td>
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<tr>
<td>Area of device</td>
<td>W*L</td>
<td>1/S²</td>
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