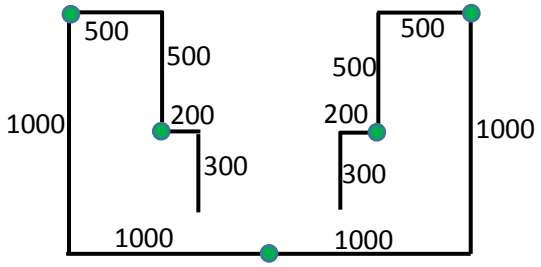
Homework #5 (clocking)

Problem #1

Consider a portion of an H tree, as shown in the figure below. It comes from the H tree shown on foil #19 from the lectures.



The wire lengths (in DU) are shown on the figure; assume all wires are 4DU wide. The green dots represent inverters.

1. Assume that the two terminuses of the H tree each drive a load of 75ff. Size the inverters, assuming a gain of 3 everywhere. To be specific, you should first compute the total load that the inverter sees, and then size the inverter to ensure that it presents 1/3 that much load as its input capacitance. Note that since we are not taking resistance into account, different inverters in the H tree will actually have somewhat different delays. Also note that the inverter at the root of the tree is a bit special, since it drives two different branches; it will thus see twice as much wire capacitance. Finally, note that, if you use the web app to calculate total loading, the "Ctotal" result box on the bottom of the app includes self-loading cap (which you don't want to use here); to remove that, just set W=0 on the driving inverter.
2. In real life, different loads have different sizes and we must deal with it. Assume now that the load on the right is actually 70ff. Resize the one inverter driving it to have a gain of 3; leave the other inverters unchanged. How much skew has this introduced into the H tree? This time, as you are computing delay, you should include wire resistance as well. Feel free to use the web calculator, as long as you also show the resulting delays for each inverter and not just the final answer.

Problem #2

Assume that we have a mother PLL distributing a 100 MHz clock. We have two daughter PLLs, one multiplying by 9 to make a 900 MHz clock and the other by 15 to make 1.5 GHz. We want to transfer data between the two daughter domains.

To use a transfer technique such as a BGF, you must turn off 6 of the 15 clocks from the 1.5GHz domain so that both domains fire 9 times every 10000 ps. Pick six pulses to turn off so as to minimize the resulting clock skew, and calculate what the skew is for your choice. Note that the convention we chose in class was that the skew is positive when the receiver clock is later than the driver clock, and that the second part of this problem will assume a path from the 900 MHz domain to the 1.5 GHz domain, so please define the sign of the skew accordingly.

To simplify the problem, assume that (since 9 and 15 have the same ratio as 3 and 5), you can divide the 10000ps period into three 3333ps periods, and treat each one identically; i.e., turn off two clock pulses from the first five, and repeat that pattern three times.

Also assume that you want to minimize the absolute value of the skew, and hence that a solution resulting in minimum skew of 0 and maximum of 100ps is worse than a solution resulting in skew between -20 and +80 ps.

Next, consider a flop-to-flop path using the above clocking scheme. Assume that the flop setup time, hold time and clk-to-Q time are all zero. If we have a path from the 900 MHz domain to the 1.5 GHz domain, we want to pick the logic delay so that the setup and hold-time constraints have an equal amount of margin. How much delay would we have to add to make this happen?

Please turn in your assignment via the Provide cgi interface. You can use any reasonable format (including writing your answers by hand and taking a picture of the page with your phone).