Homework #4 (gate sizing)

Problem #1. Consider the delay model that we've used for our sizing unit, where

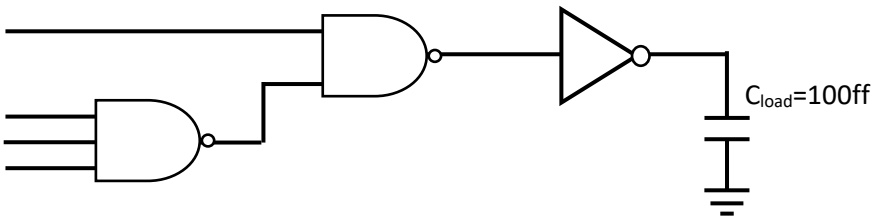
- Device resistance $R = k_{devR}\, L/W$ (where k_{devR} has units of ohms)
- Self-loading capacitance of a device $C_{self} = k_{self}$ *W (where k_{self} has units of ff/DU)
- Delay $D = R*(C_{self} + C_{load})$
- $C_{in} = k_{gate}$ * L*W (where k_{gate} has units of ff/DU^2). I.e., this is the input capacitance of a gate as a function of the gate's device sizes (the sum of the N-device and P-device gate areas on any of the gate's inputs).

Note that for simplicity, we've ignored wire resistance. Consider a simple inverter driving a fixed loading capacitor. Prove that, for a given delay D:

1. The width W is directly proportional to C_{load}: i.e., $W = k*C_{load}$ for some constant k that depends on D.
2. The gain of the gate (C_{load}/C_{in}) is constant; it does not depend on the load.
3. The self-loading fraction $C_{self}/(C_{self}+C_{load})$ is constant; it does not depend on the load.

Problem #2.

Consider the network shown below. Size it assuming that all transistors have L=2DU and that all inverters have a gain of 3. At this gain, inverters have a delay of roughly 45ps, and $W_{n,eff}$ = (2.8DU/ff) * C_{load}. Assume that device input capacitance C_{in}=.02 ff/DU^2. Size the NAND gates to have roughly (i.e., other than self loading) the same 45ps delay as the inverters, as we discussed in class (this will result in them having a gain less than 3).



Please turn in your assignment via the Provide cgi interface. You can use any reasonable format (including writing your answers by hand and taking a picture of the page with your phone).