

A Framework for Simulating Heterogeneous Virtual Processors 32nd Annual Simulation Symposium, System Simulation session April 12, 1999

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Design Patterns Generate Behavior across Media

The question is whether it is possible to write down rules or patterns for architecture—and software and art—so that ordinary people can follow the rules or patterns and, by the nature of the patterns and using only the abilities of ordinary people, beauty is generated. If this happens, then the rules or patterns are generative, which is a rare quality.

— Richard Gabriel, Patterns of Software

LUxWORKS *luxdbg* simulator / debugger applies three design patterns across system layers:

- Build and extend abstract virtual processors.
- Build reflective entities.
- Build a covariant extensible system.

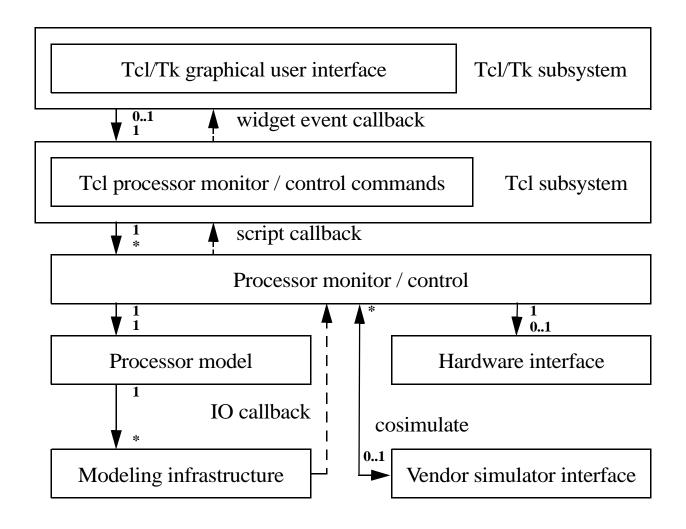
Universal Design Patterns constitute a lingua franca

"I can go anywhere in the system and recognize what is going on."

a processor designer using LUxWORKS framework.

Extension medium (meta-data, extension language) Aggregate medium (construction process, modules) Primitive medium (domain building blocks) Primitive medium (domain building blocks) Primitive medium (domain building blocks)

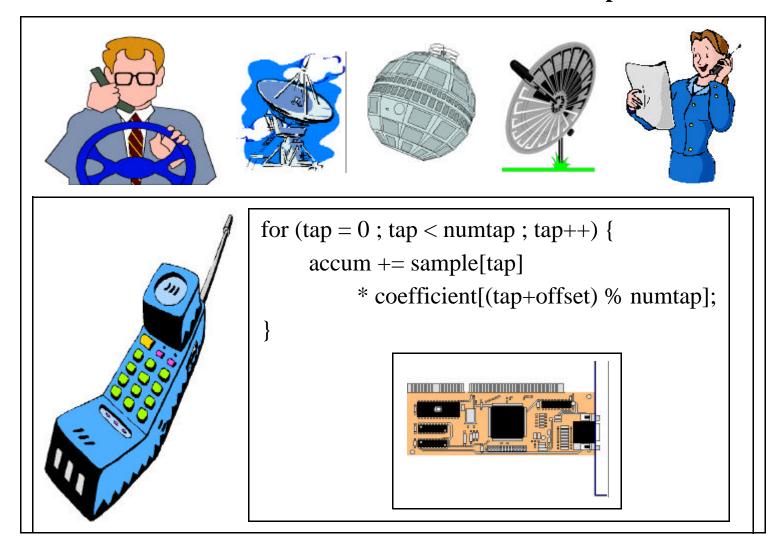
Layers of the LUxWORKS Framework



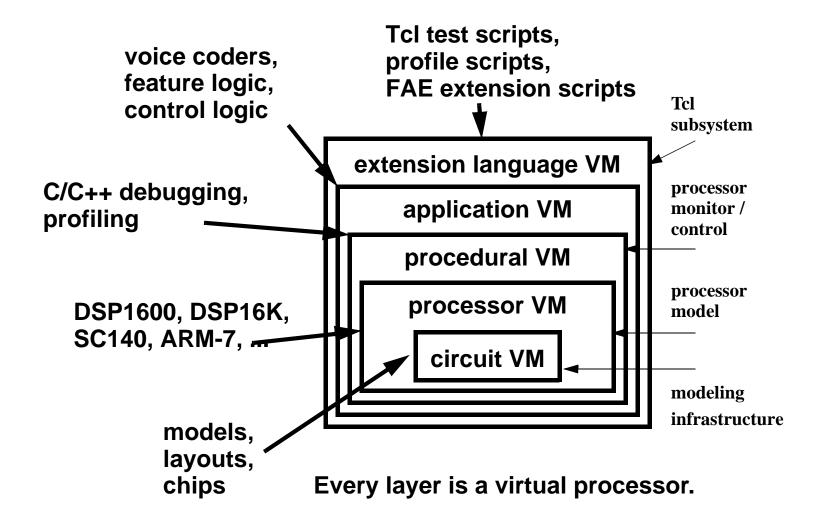
Modules of the LUxWORKS Framework

BEHAVIORAL API INST PHASE DSP16K A st of 20-bit with A st of bits in the la * 32-bit word A cl-od(0) DSP1600 Tcl/ Embed-**ALGORITMIC API** ded **LUxDBG** func(input1[], input2[], output[]) API TVM API COEF DATA Scheduler DSP1600 DSP16K Finite Arithmetic effects TAP Mgr TAP Mgr **Chain Manager** DATA JTAG Driver

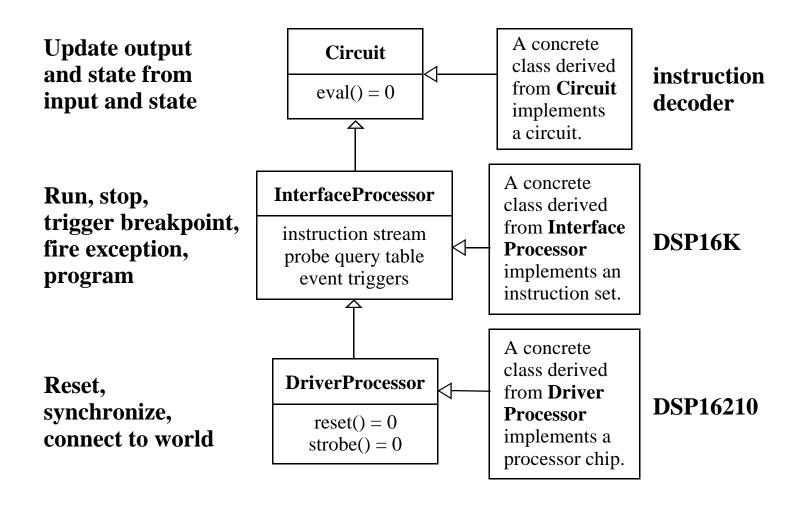
PATTERN #1: Build and extend abstract virtual processors.



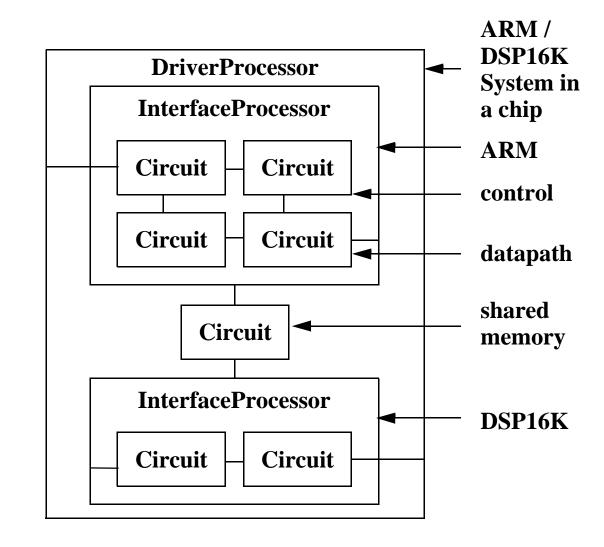
PATTERN #1: Build and extend abstract virtual processors.



What can one do with an Abstract Virtual Processor?

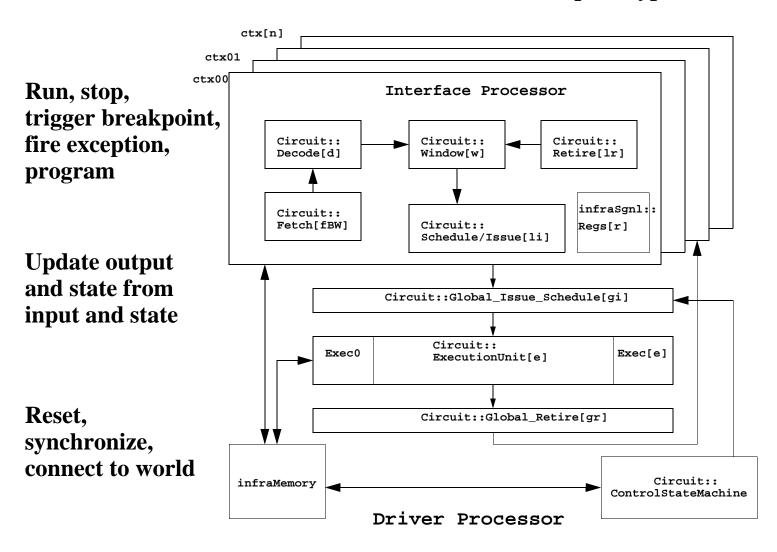


How can one combine Abstract Virtual Processors?

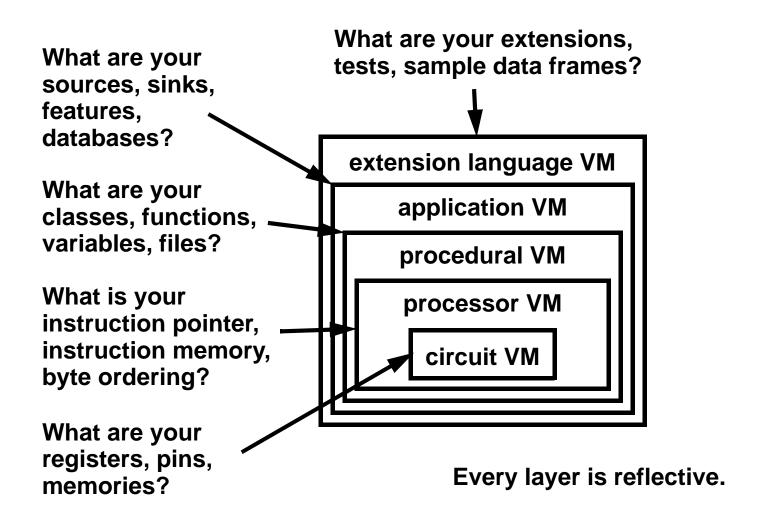


Connect them at construction time.

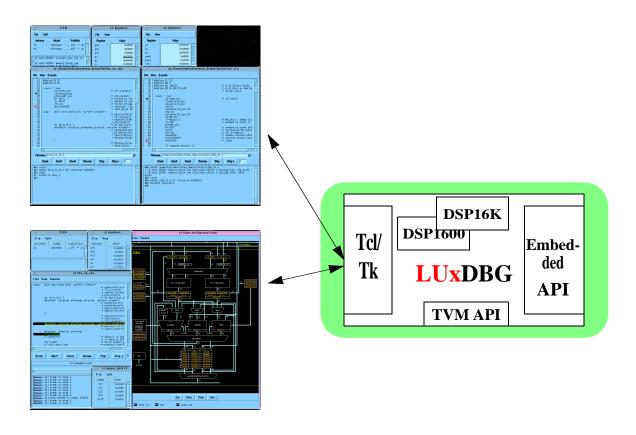
Abstract Virtual Processors for architectural prototypes



PATTERN #2: Build reflective entities.



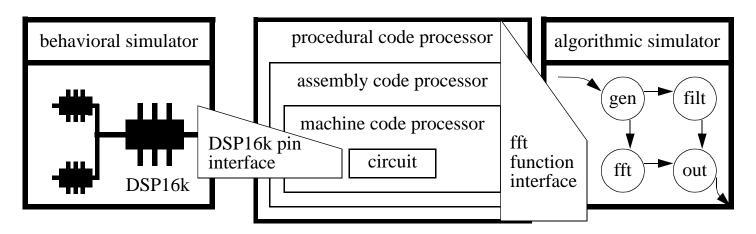
Reflective processors yield configurable tools.



GUI uses relational and hierarchical mega-widgets. GUI configures itself to processors & programs at run time.

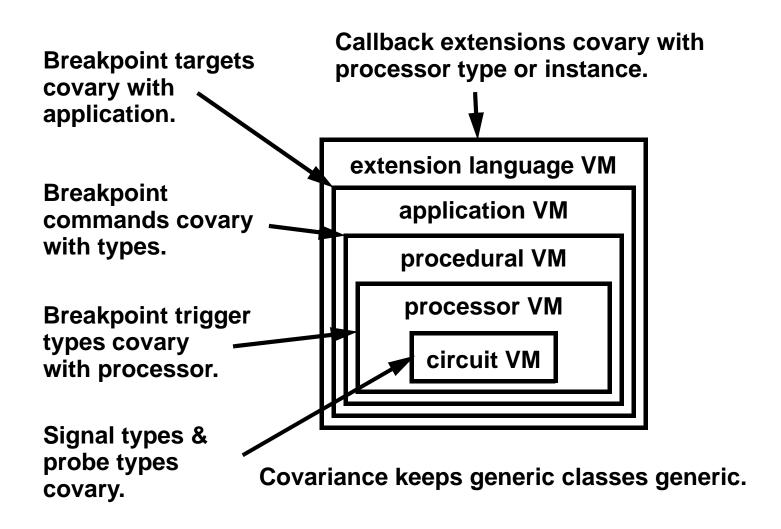
Reflective processors yield configurable bridges to tools.

Behavioral simulator bridge queries simulator & LUxWORKS model for pin & clock timing bindings.

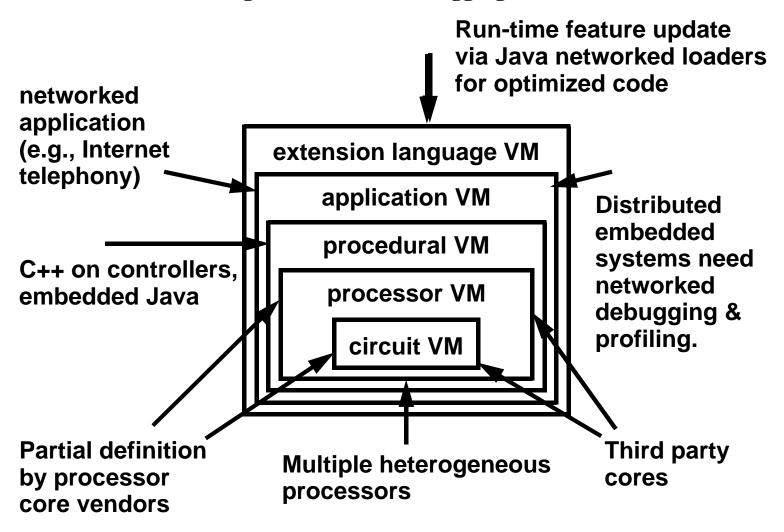


Algorithmic simulator bridge queries simulator & LUxWORKS symbol table for function & parameter bindings.

PATTERN #3: Build a covariant extensible system.



Forces driving simulation & debugging architectural evolution



Conclusions

- Virtual Processor pattern gives universal ability to trigger events, reset, execute, halt execution and deliver break events to clients.
- Universal inheritance from Virtual Processor base classes Circuit and Interface Processor supports on-the-fly composition of processors into higher-order system simulations.
- Universal reflection allows tools and tool bridges to configure themselves to processors and programs at execution time.
- Processor-oriented covariance allows tool capabilities to vary with process-specific support without perturbing generic tool code.
- Current direction is unification of simulation, embedded hardware execution & real-time operating system task execution.
- Increase in support for networked simulation & debugging.